Exhibit 12

Paper No. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 9,318,160

Issued: April 19, 2016

Filed: July 21, 2014

Inventor: Hyun Lee

Title: Memory Package with Optimized Driver Load and Method of Operation

Inter Partes Review No. IPR2022-01427

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,318,160

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1022	Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008)
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1026	U.S. Patent Application Publication No. 2006/0277355 to Ellsberry *et al.* (published Dec. 7, 2006)
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CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a	1. A memory package, comprising:
1.b	data terminals and control terminals;
1.c	stacked array dies including a first group of array dies and a second group of at least one array die;
1.d.1	first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
1.d.2	the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
1.e.1	a control die comprising
1.e.2	first data conduits between the first die interconnects and the data terminals, and
1.e.3	second data conduits between the second die interconnects and the data terminals,
1.e.4	the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies,
1.e.5	the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.
2	The memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects, and wherein the second driver size is larger than the first driver size.
3.a	The memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects, and
3.b	wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies.

Ref. #	Listing of Challenged Claims
4	The memory package of claim 1, wherein the first driver size and the second driver size are related to a load on the first driver and a load on the second driver.
5	The memory package of claim 1, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via the control terminals.
6.a	A memory package, comprising:
6.b	data terminals and control terminals;
6.c	stacked array dies including a first group of array dies and a second group of at least one array die;
6.d.1	first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
6.d.2	the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
6.e	wherein the second die interconnects are longer than the first die interconnects, and
6.f	wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies.
7.a	The memory package of claim 6, further comprising: a control die comprising
7.b.1	first data conduits between the first die interconnects and the data terminals, and
7.b.2	second data conduits between the second die interconnects and the data terminals,
7.c.1	the first data conduits including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies,

Ref. #	Listing of Challenged Claims
7.c.2	the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.
8	The memory package of claim 7, wherein the second driver size is larger than the first driver size.
9	The memory package of claim 7, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via one or more second terminals of the plurality of terminals.
10.a	A memory module operable in a computer system with a system memory controller, comprising
10.b	a register device configured to receive input command/address signals from the system memory controller and to output control signals; and
10.c	a plurality of DRAM packages, each DRAM package comprising:
10.d	data terminals via which the DRAM package communicate data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device;
10.e	stacked array dies including a first group of array dies and a second group of at least one array die;
10.f.1	die interconnects including first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
10.f.2	the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
10.g.1	a control die including
10.g.2	first data conduits between the first die interconnects and data terminals, and
10.g.3	second data conduits between the second die interconnects and the data terminals,

Ref. #	Listing of Challenged Claims
10.h.1	the first data conduits including first drivers each having a first driver size, the second data conduits including second drivers each having a second driver size different from the first driver size,
10.h.2	the first drivers to drive first write data signals received from the system memory controller to one of the first group of array dies, the second drivers to drive second write data signals received from the system memory controller to one of the second group of at least one array die.
11	The memory module of claim 10, wherein the control die receives the control signals and further includes a control circuit to control respective states of the first data conduits and the second data conduits in response to the control signals.
12	The memory module of claim 11, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduits and the second data conduits.
13	The memory module of claim 11, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduits and the second data conduits.
14.a	The memory module of claim 10, wherein the control signals include address signals and
14.b	the control die provides the address signals to the plurality of array dies.
15.a	The memory module of claim 10, wherein the input command/address signals include first chip select signals,
15.b	wherein the register device is configured to perform rank multiplication by generating second chip select signals from at least some of the input command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies, and
15.c	wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies.

Ref. #	**Listing of Challenged Claims**
16.a	The memory module of claim 10, wherein the control signals include output command/address signals derived from the input command/address signals, the output command/address signals including first chip select signals,
16.b	wherein the control die is further configured to perform rank multiplication by generating second chip select signals from at least some of the output command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies, and
16.c	wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies.
17	The memory module of claim 10, wherein the first driver size and the second driver size are related to a first load on the first driver and a second load on the second driver.
18	The memory module of claim 10, wherein the control signals include command/address signals, and the control die includes buffers to control the timing of the command/address signals.
19	The memory module of claim 10, wherein the control die includes data buffers to control the timing of the data signals.
20	The memory module of claim 10, wherein the first group of array dies include a greater number of array dies than the second group of at least one array die.

I. PETITIONER'S MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

The real parties in interest are the Petitioner, Samsung Electronics Co., Ltd., and Samsung Semiconductor, Inc.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 9,318,160.

The following proceedings are currently pending:

- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. amended complaint filed May 3, 2022)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-01428 (U.S. Patent No. 8,787,060)
- U.S. Application No. 17/694,649

C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

Lead Counsel is Eliot D. Williams (Reg. No. 50,822), DLSamsungNetlistIPRs@BakerBotts.com, (212) 601-7255, Baker Botts L.L.P., 30 Rockefeller Plaza, New York, NY 10112.

Backup Lead Counsel are:

- Theodore W. Chandler (Reg. No. 50,319),

  DLSamsungNetlistIPRs@BakerBotts.com, (213) 202-5702

- Ferenc Pazmandi (Reg. No. 66,216),

  DLSamsungNetlistIPRs@BakerBotts.com, (415) 291-6255

- Michael E. Knierim (Reg. No. 78,268),

  DLSamsungNetlistIPRs@BakerBotts.com, (212) 408-2584

- Brianna L. Potter (Reg. No. 76,748),

  DLSamsungNetlistIPRs@BakerBotts.com, (650) 739-7556

The fax number for lead and backup counsel is (650) 739-7699.

D. Service Information (37 C.F.R. § 42.8(b)(4))

Service information is provided in the designation of counsel above.

Petitioner consents to service of all documents via electronic mail to DLSamsungNetlistIPRs@BakerBotts.com.

II. INTRODUCTION

Petitioner respectfully requests trial on claims 1-20 of U.S. Patent 9,318,160 ("160 Patent") (EX1001) based on grounds not considered during prosecution.

III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Standing (§42.104(a))

Petitioner certifies that the 160 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the 160 Patent claims on the grounds identified below.

B. Identification of Challenge (§42.104(b))

Petitioner challenges claims 1-20 of the 160 Patent as follows:

Ground	Claims Challenged	35 U.S.C. §	References
1	1-20	103(a)	Kim+Rajan+Wyman
2	1-20	103(a)	Riho+Rajan+Riho2

Petitioner's proposed claim constructions and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon is listed above on page vi.

IV. RELEVANT INFORMATION CONCERNING THE CONTESTED PATENT

A. Effective Filing Date of the 160 Patent

All the prior art in the Grounds above predates November 3, 2010, when the provisional application for U.S. Patent No. 8,787,060 (the "060 Patent") was filed (to which the 160 Patent claims priority), but to the extent it matters, the claims of the 160 Patent do not appear to have support in any application filed before ***November 3, 2011***. EX1003, ¶¶47-59. For example, all the independent claims

require "*first*" and "*second*" "*group[s] of … array die[s]*" in a single memory package, but the provisional does not disclose that. EX1005, ¶¶[0006]-[0012], Fig.3 (below); EX1003, ¶¶51-53.

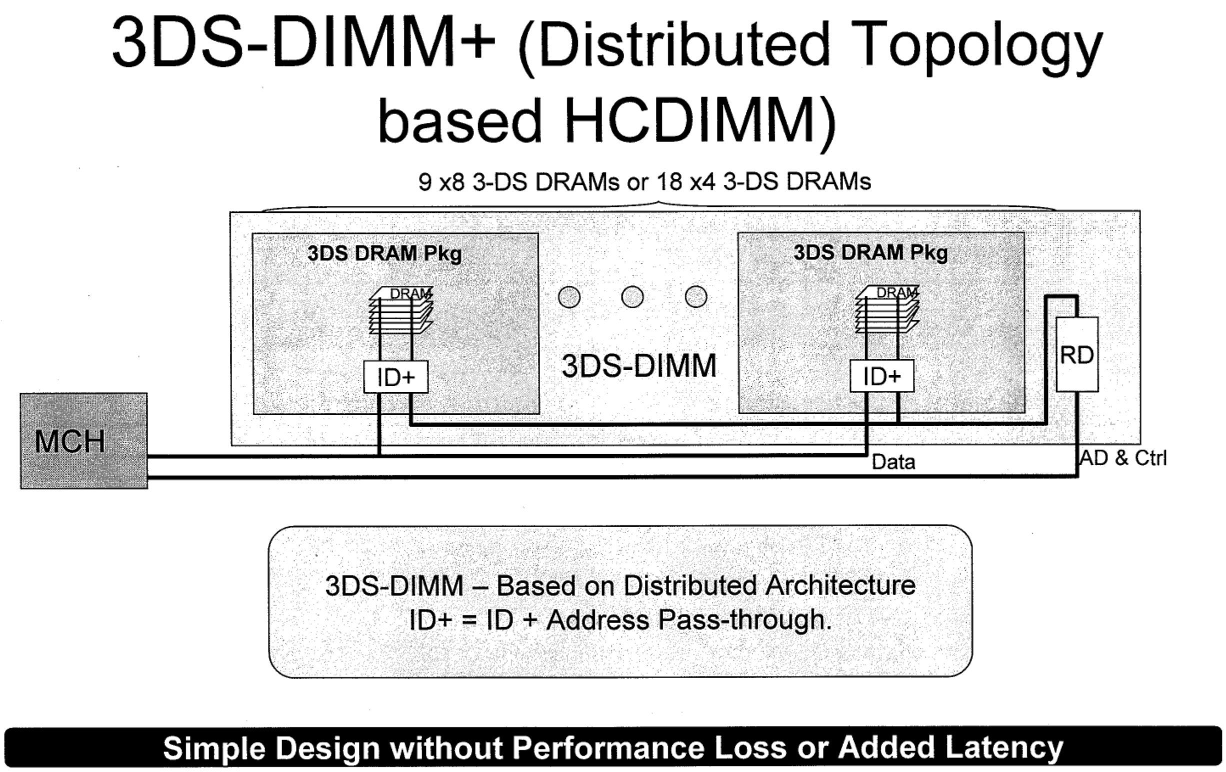


Figure 3

Furthermore, the provisional does not disclose "*first*" and "*second*" "*die interconnects*" in "*electrical communication*" with one group of array dies but not the other group, as required by all the independent claims, and does not disclose "*respective states*" of "*data conduits*" as required by claims 5, 9, and 11. EX1005, Figs.1-3; EX1003, ¶¶54-59.

B. Person of Ordinary Skill in the Art ("POSITA")

A POSITA in the field of the 160 Patent in 2010 and 2011 would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. EX1003, ¶60. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of DRAM and SDRAM memory devices and memory modules, including standardized interfaces for interfacing with a memory controller and other parts of a computer system. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used in stacked memory devices, including structure and circuitry in JEDEC-proposed three-dimensional stacking and circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers and their corresponding electrical loads. *Id.*

C. Background Technology

1. JEDEC Standards

As recognized by the provisional application, EX1005, ¶¶[0004-05], a POSITA would have been familiar with the JEDEC standards for memory devices

and memory modules. EX1003, ¶¶131-133; EX1023, p.9 & Fig.16; EX1022, pp.332-35, 318-20. For example, a POSITA would have understood that DDR SDRAM memory devices were already standardized by JEDEC. EX1015, 8:6-15; EX1016, ¶[0027]; EX1003, ¶131. Moreover, a POSITA would have understood that JEDEC had standardized memory modules and corresponding interface circuits such as "a register, an AMB, a buffer, or the like." EX1015, 4:20-24; EX1003, ¶131. Examples of relevant standards include the JEDEC standard for DDR3 memory devices, EX1019-21, and the JEDEC specification for GDDR4 memory devices, EX1035.

2. <u>Electrical Load and Drivers</u>

A POSITA would have been familiar with basic concepts like electrical loads of circuitry used in stacked memory devices and corresponding driving requirements to drive the load of such circuitry. EX1001, 2:10-17 (acknowledging known tradeoff between driver size, load, space, and power); EX1003, ¶134. For example, the greater the "fan-out," the greater the capacitive loading, and thus the greater the propagation delay, as shown below. EX1030, pp.132-138, Fig.3.55 (below); EX1003, ¶135.

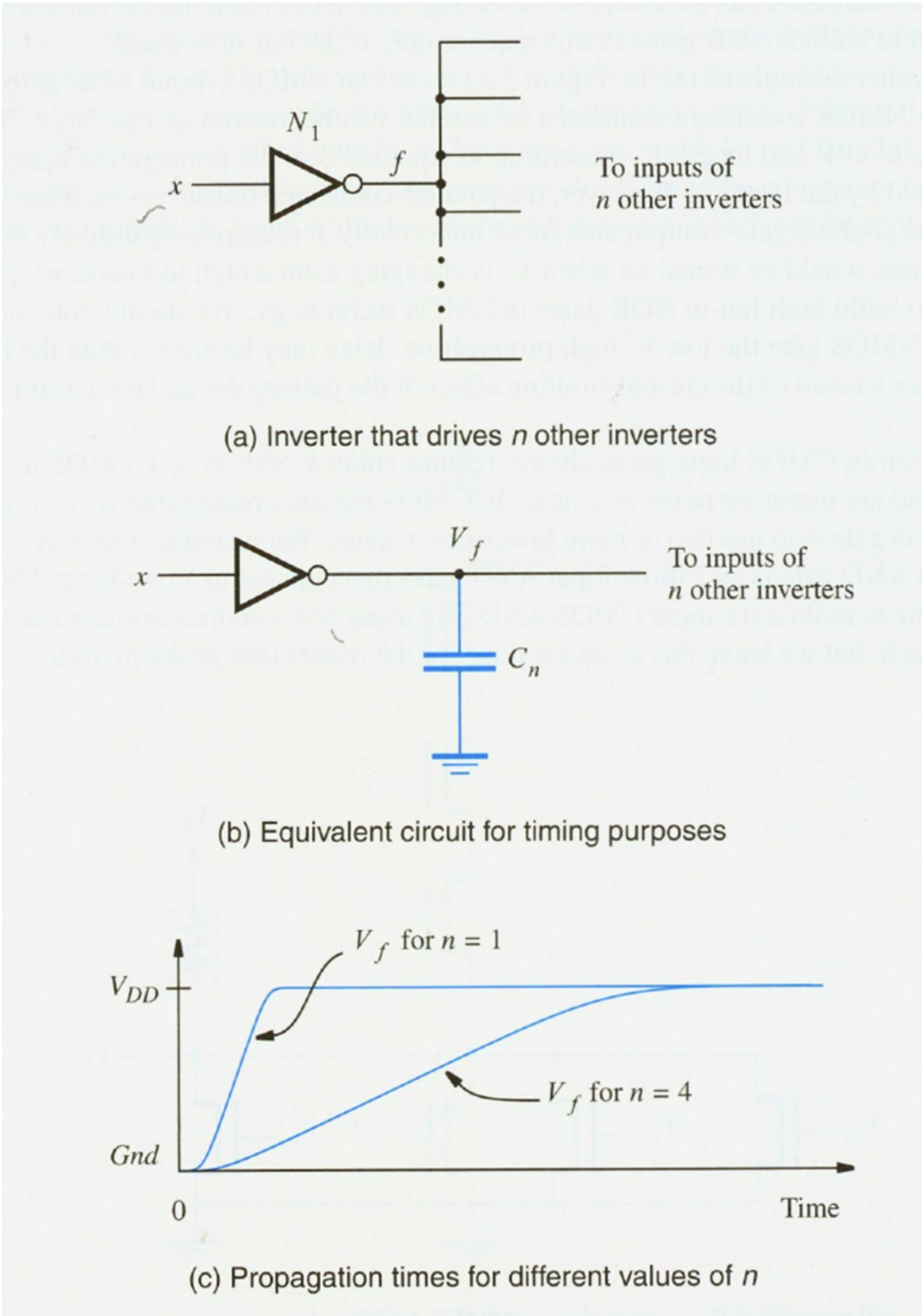


Figure 3.55 The effect of fan-out on propagation delay.

A POSITA would have understood that buffers (such as tri-state buffers) were often used to improve performance when driving a large capacitive load, and

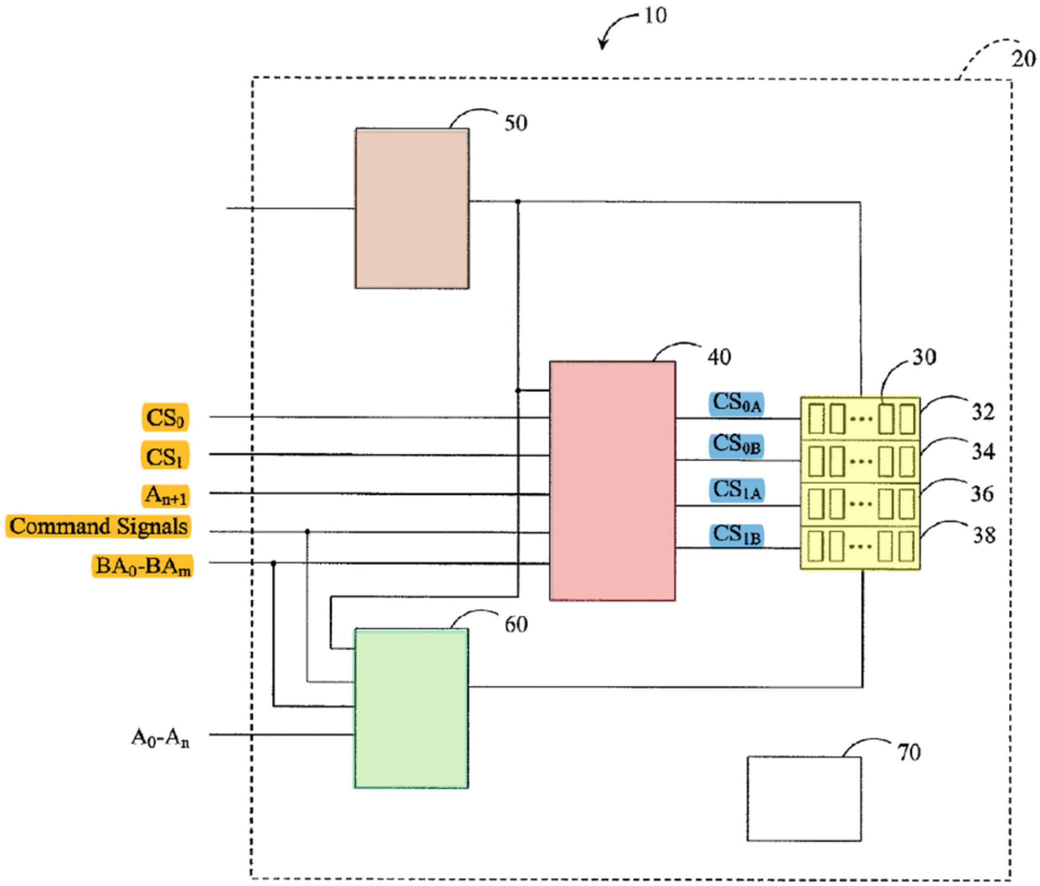
that "[b]uffers can be created with different amounts of *drive capability*." EX1030, pp.135-138; EX1003, ¶136.

3. <u>Rank Multiplication</u>

As admitted by the 160 Patent, a POSITA also would have been familiar with "rank multiplication"—e.g., where a memory module can appear to the computer system as if it has two ranks of higher density (and more expensive) memory devices complying with the JEDEC standard, when it physically has four ranks of lower density (and less expensive) memory devices—which can result in substantial cost savings, providing a motivation to implement the technique in a wide range of memory packages and memory modules. EX1001, 22:22-24 ("Embodiments of rank multiplication are described in greater detail in U.S. Pat. Nos. 7,289,386 ["the 386 Patent," EX1028, 4:47-5:10, 32:58-33:16] and 7,532,537 [EX1031] ...."); EX1041, 2:15-19; EX1015, 6:30-7:67; EX1003, ¶137.

As illustrated in Figure 1A (below) of the prior-art 386 Patent, rank multiplication involves mapping chip select signals (e.g., CS_0, CS_1, orange) and address signals (e.g., A_{n+1}, orange) received from a system controller complying with the JEDEC standard into ***more*** chip select signals (CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}, blue) to control the higher number of ranks of memory devices (yellow) on the module. EX1028, 2:34-38, 5:11-50, 6:63-8:45, Fig.1A; EX1003, ¶¶138-139.

Figure 1A:



More ranks would result in more load, however, so the prior-art 386 Patent explains that an isolation device (e.g., 120 below) should be used to reduce the electrical load created by the additional ranks of memory devices, and to avoid certain data collisions. EX1028, 24:41-56, 26:12-19, Fig.6D (below); *see also* EX1031, 6:48-62; EX1003, ¶139.

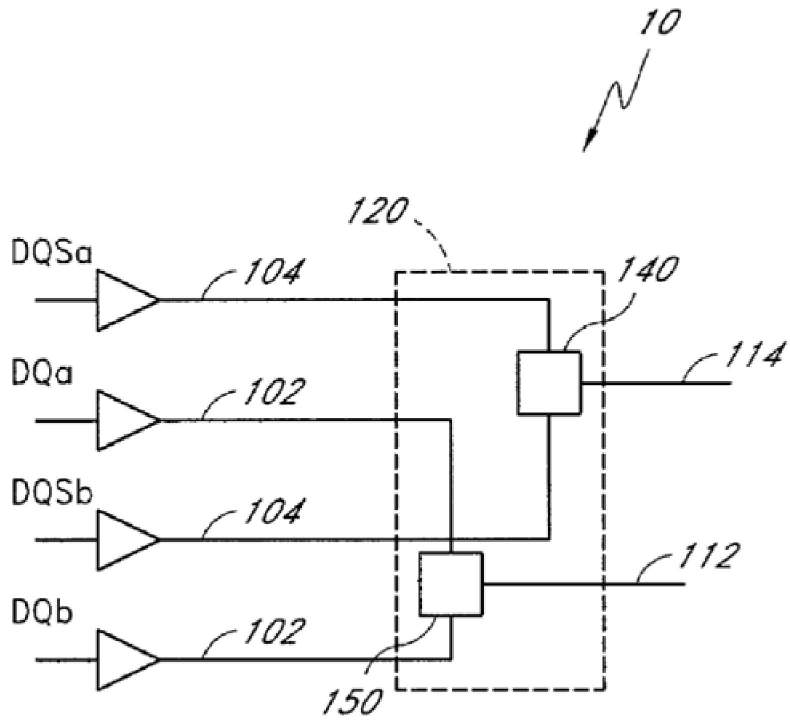


FIG. 6D

While the prior-art 386 Patent discloses rank multiplication implemented in a separate controller (the register), *see* EX1028, 5:42-48, POSITAs would have known that it could ***also*** be implemented within a single memory package on the control die, or in both locations, *see* EX1015, 6:30-7:67; EX1041, 2:15-19; EX1001, 18:26-62, Fig.7 (below, showing prior-art module implementing rank multiplication in both the module controller 712 and the memory package control chip 722); EX1003, ¶140.

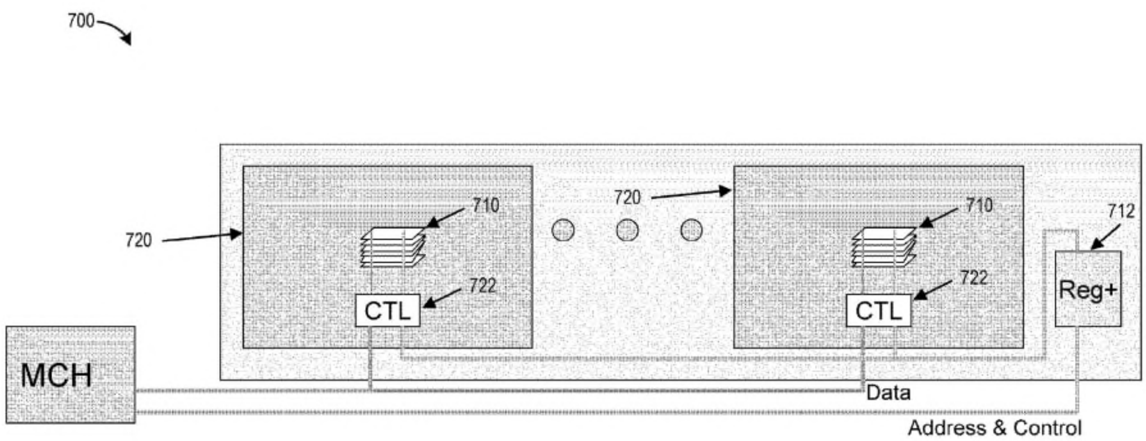


FIG. 7

D. The 160 Patent

1. <u>Technical Overview</u>

The 160 Patent "relates to memory devices and memory modules …. specifically … [ways] for reducing the load of drivers of memory packages included on the memory modules." EX1001, 1:20-23.

The 160 Patent admits as prior art the memory package designs depicted in Figures 1A and 1B (annotated below),[1] which include, for example, "array dies 160 [(yellow)] and a control die 170 [(green)] that … [includes] a driver 184 that drives data signals to each of the array dies 160 along a corresponding die

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[1] Unless stated otherwise, all emphasis in quotes and color annotations in figures have been added.

interconnect 182 [(light green)].” EX1001, 1:32-35, 1:65-2:6, Fig.1B; EX1003, ¶61.

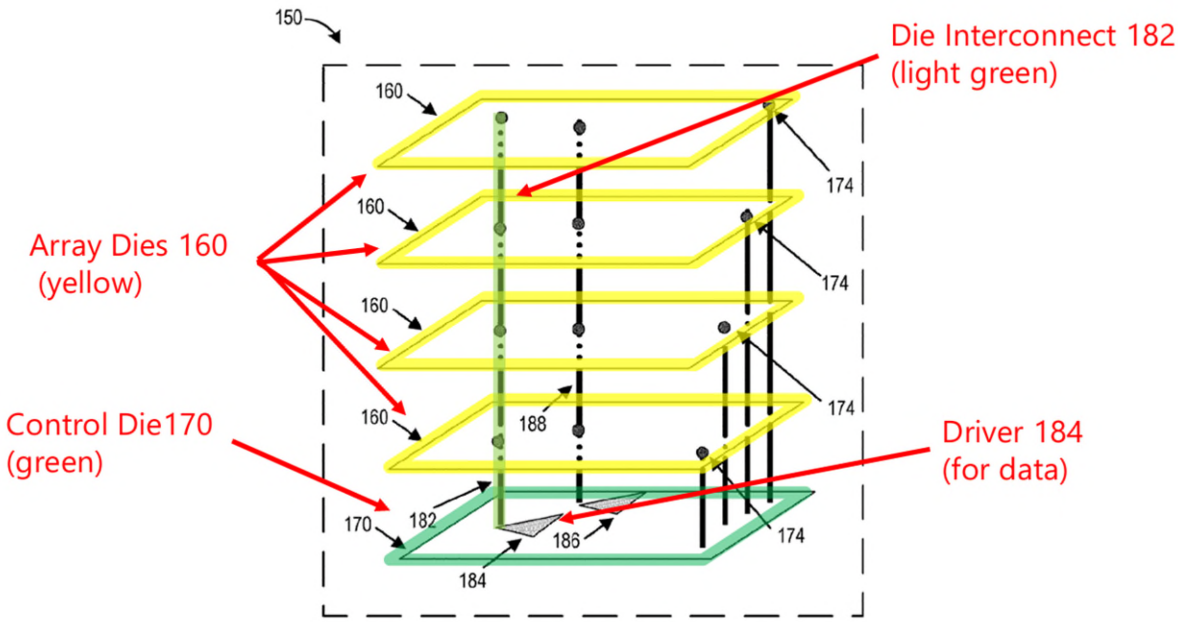
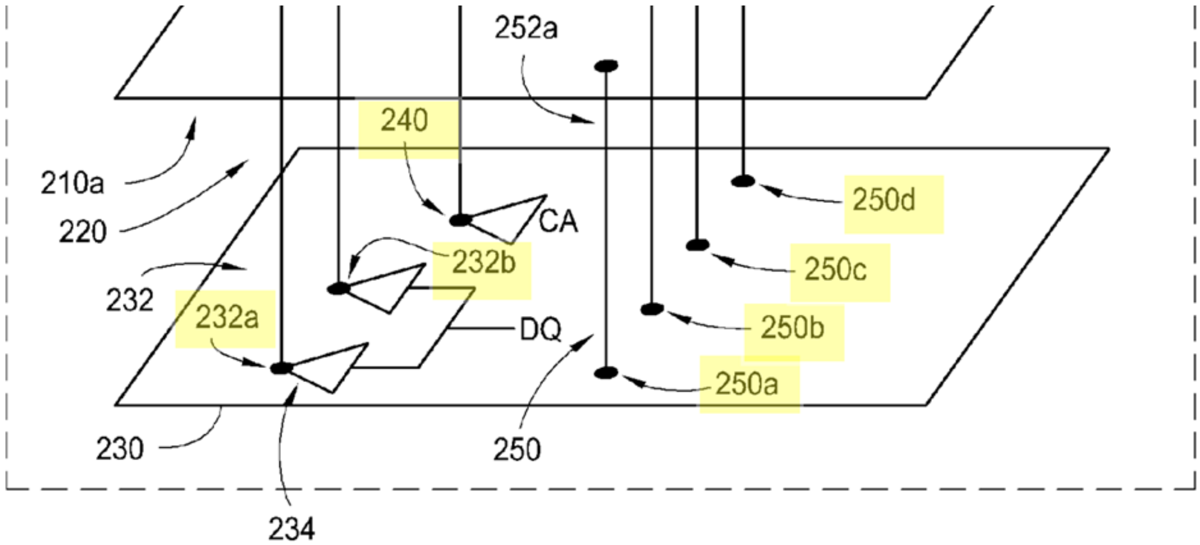


FIG. 1B

The 160 Patent teaches that each die interconnect has a corresponding “conduit” (e.g., 232a below), configured to transmit a signal to the die interconnect, and which may include a driver. EX1001, Fig.2, 6:51-65, 9:31-63, 21:3-5; EX1003, ¶62.



As illustrated by Figure 2 (below), the 160 Patent purports to improve upon the prior art (e.g., Figure 1B) by replacing ***one*** data driver (e.g., driver 184 in Figure 1B) with ***two*** or more drivers 234 coupled to the same DQ data terminal, each driving the data signal through a respective die interconnect (220a, 220b) in electrical communication with a ***subset*** of the array dies, thereby reducing the overall load of each data conduit. EX1001, 1:21-23, 1:65-2:6, 2:10-17, 7:12-8:21, Fig.2; EX1003, ¶¶61-63.

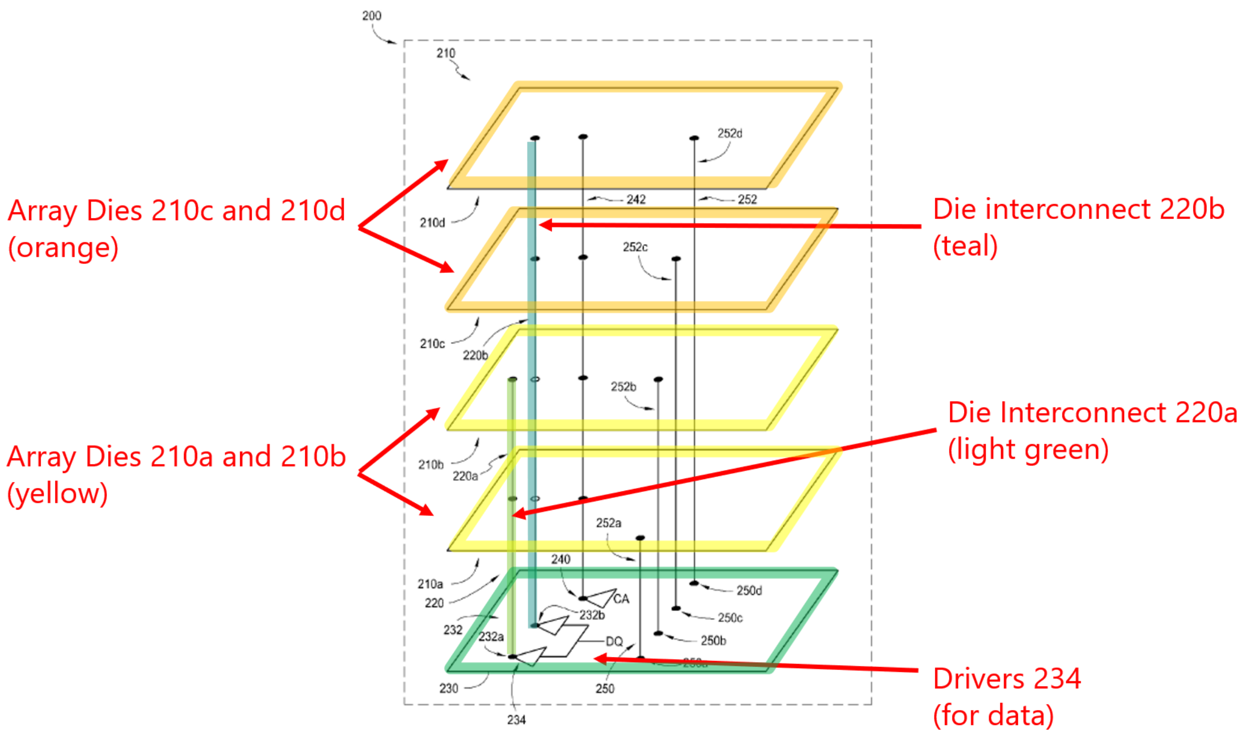


FIG. 2

In Figure 2, for a given data bit (e.g., D0), die interconnect 220a (light green) may be in electrical communication with data ports from array dies 210a and 210b (yellow) (as illustrated by darkened circles) and not in electrical communication with data ports from array dies 210c or 210d (orange), while die interconnect 220b (teal) may be in electrical communication with data ports from array dies 210c and 210d and not 210a and 210b, even though die interconnect 220b may pass through these array dies (as illustrated by unfilled circles), "e.g., through through-holes or vias of array dies 210a and 210b." EX1001, 5:66-6:4, 6:12-18; EX1003, ¶64.

The 160 Patent further discloses selecting the number of array dies connected to a die interconnect to reduce the difference between the loads on the different data conduits. For example, assuming the load of each array die is 1L, and the load of each segment of the die interconnect is 0.25L, a die interconnect in electrical communication with 8 array dies (like in the prior art) would result in a maximum load of 10L. EX1001, 7:25-32, 12:46-13:18; EX1003, ¶65. But by increasing the number of die interconnects and varying the number of array dies in electrical communication with each die interconnect, the load for each data conduit can be reduced to 2.5L to 3.0L as shown in Table 1 below, allowing for smaller drivers. EX1001, 10:21-58, 12:46-13:18, Fig.3 (below) & Table 1 (below, illustrating "the deviation in load from the conduits having the highest load value"); EX1003, ¶65.

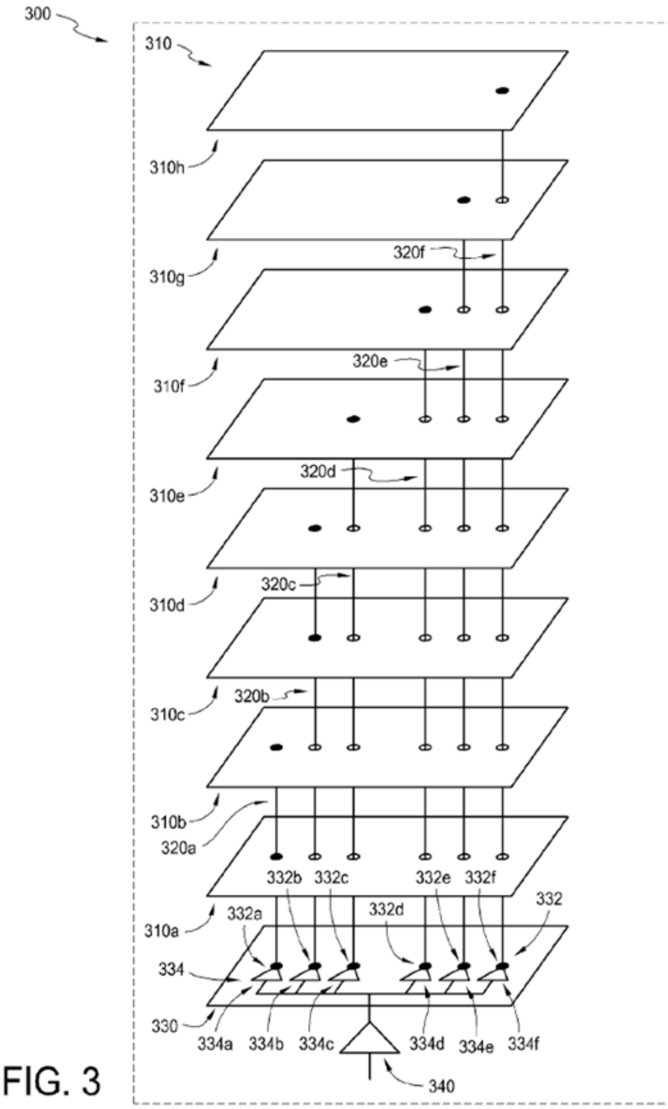


FIG. 3

TABLE 1

Conduit	Number of Array Dies	Number of Die Interconnect Segments	Capacitive Load	Deviation from Maximum Load
332a	2	2	2.5 L	0.5
332b	2	4	3 L	0
332c	1	5	2.25 L	0.75
332d	1	6	2.5 L	0.5
332e	1	7	2.75 L	0.25
332f	1	8	3 L	0

2. Prosecution History

During prosecution of the 060 Patent (of which the 160 Patent is a continuation), the independent claims (and others) were rejected as anticipated by Rajan137 (EX1011) (different than the Rajan reference relied upon in this Petition). EX1002, pp.238-48, 433-443; EX1003, ¶¶68-72. In response, Patent Owner argued that Rajan137 "merely stacks DRAM circuits 206A-D, which are different from array dies," and "[a]s a result, Rajan[137]'s buffer chip 202 operates very differently" from the claimed control die. EX1002, pp.465-66; EX1003, ¶73. The Examiner allowed the claims, with minor Examiner's amendments, but without any stated reasons for allowance. EX1002, pp.474, 478-80; EX1003, ¶¶74-75. A series of later-filed applications claiming priority to the 060 Patent, including the application resulting in the 160 Patent, were allowed after the filing of terminal disclaimers, but without any further discussion of prior art. EX1006-EX1010; EX1003, ¶¶76-106.

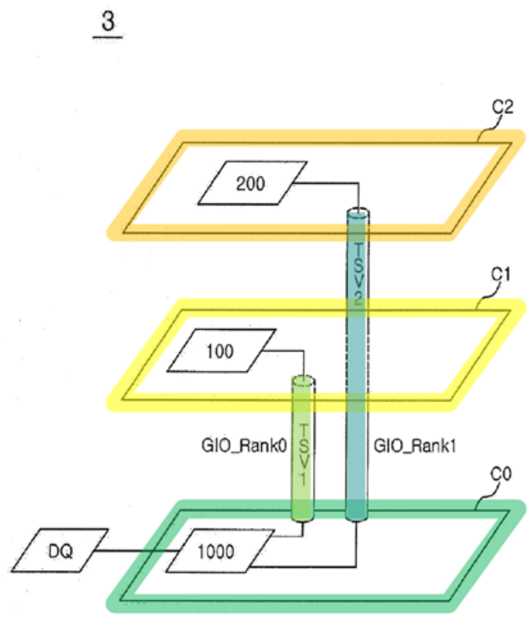
V. OVERVIEW OF THE PRIOR ART

A. Kim (EX1014)

U.S. Patent Publication No. 2011/0103156 ("Kim"), filed in 2009 and published May 5, 2011, is prior art at least under §102(e). EX1014, 1. Kim discloses one or more main chips, e.g., C0 (green) and two or more slave chips, e.g., C1 (yellow) and C2 (orange), the chips being connected by through-silicon vias (TSVs) (light green and teal, respectively). EX1014, ¶¶[0047-48], Fig.5

(below); EX1003, ¶¶114-117. Main chip C0 includes an input/output section (1000) shared by C1 and C2, designated as the first rank, Rank0, and the second rank, Rank1, respectively, and the first chip-select signal CS0 and the second chip-select signal CS1 become signals for selecting C1 and C2, respectively. EX1014, ¶[0049]; EX1003, ¶116.

FIG.5



B. Rajan (EX1015)

U.S. Patent No. 8,041,881 ("Rajan"), filed in 2007 and issued October 18, 2011, is prior art at least under §102(e). EX1015, 1. Rajan discloses making high-capacity memory using low-cost memory chips, e.g., using stacked DRAM memory chips (yellow, orange) and a buffer chip (green) for interfacing with a host system, and connecting the stacked DRAM chips and the buffer, e.g., using two

data busses (light green and teal). EX1015, 1:51-60, 4:48-50, Fig.4 (below); EX1003, ¶¶118-119.

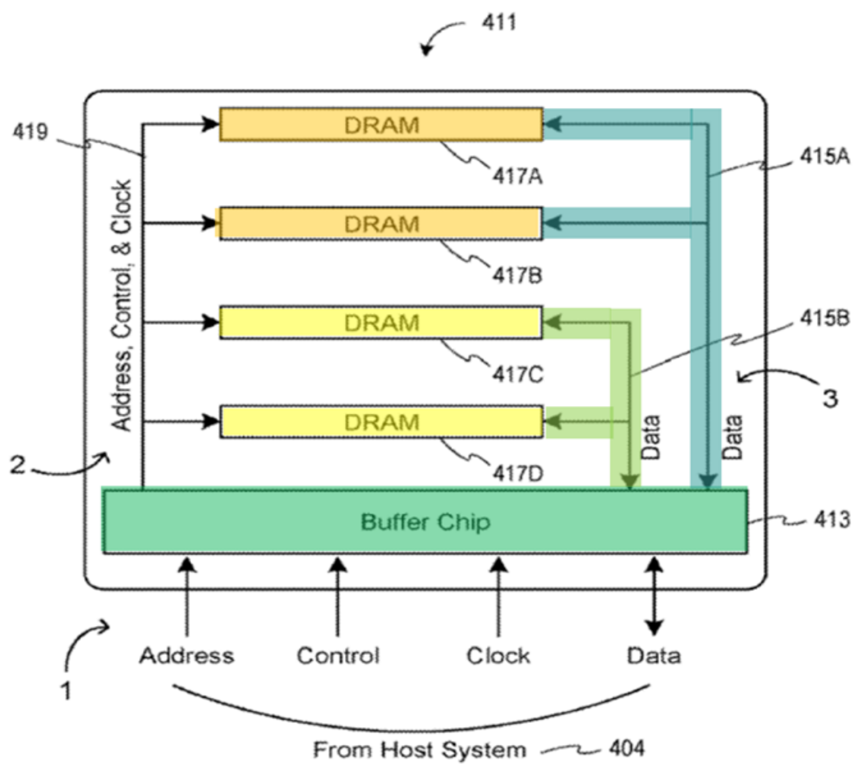


FIG. 4

Rajan further discloses its interface with the host can comply with JEDEC standards. EX1015, 4:20-24, 14:11-18, Fig.18 (below); EX1003, ¶120.

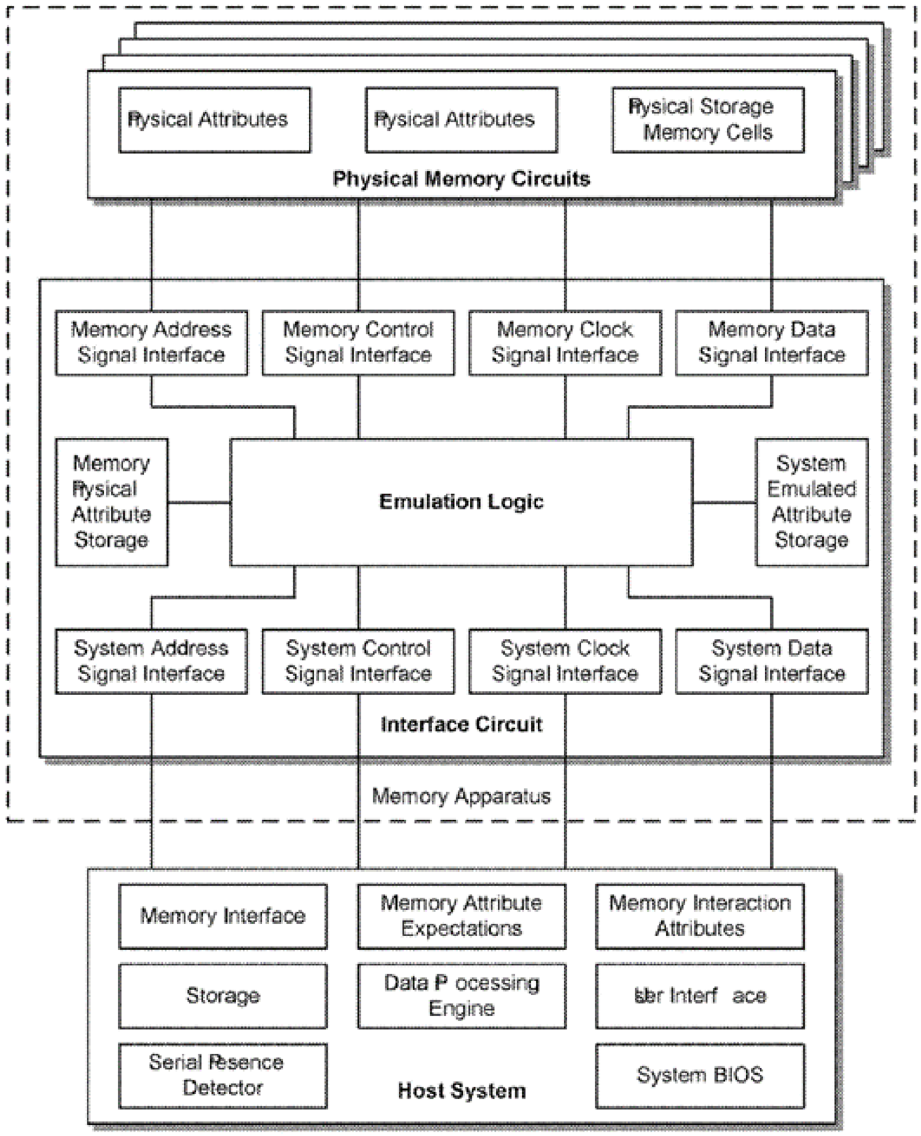


FIG. 18

C. <u>Riho</u> (EX1016)

U.S. Patent Publication No. 2011/0026293 ("<u>Riho</u>"), filed July 16, 2010, and published February 3, 2011, is prior art at least under §102(e). EX1016, 1. <u>Riho</u> discloses a memory package with a control chip (logic LSI chip 20, green) and stacked SDRAM chips (D0-D15), organized into pairs, connected to the control chip by through-silicon vias (TSVs), "to reduce by half the load … as compared

with the case where the SDRAM chips are not divided into groups." EX1016, ¶[0103], Figs.1-2 (below); EX1003, ¶¶121-124.

FIG. 1

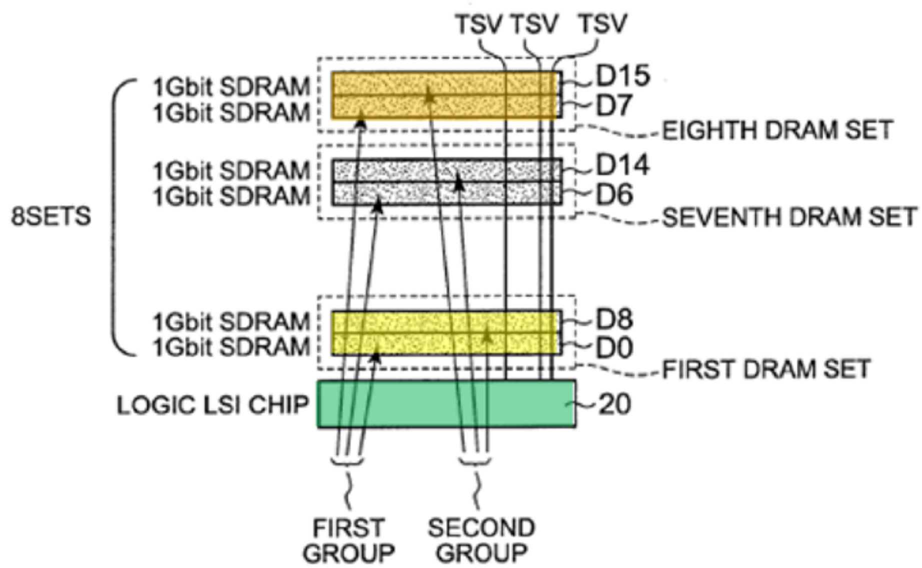
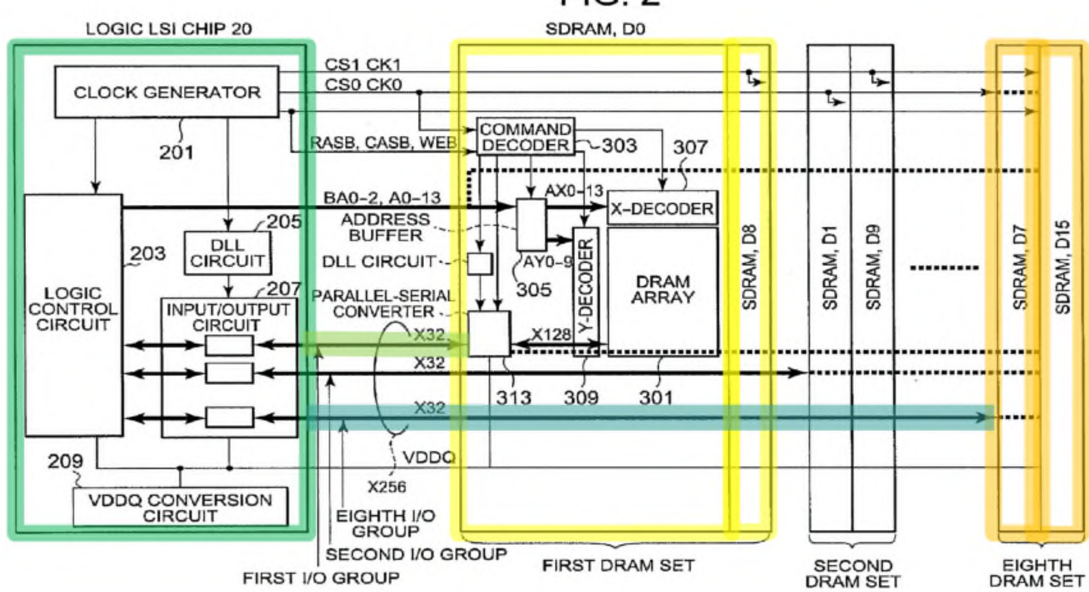


FIG. 2



D. Wyman (EX1017)

U.S. Patent No. 7,969,192 ("Wyman"), filed March 26, 2010, and issued June 28, 2011, is prior art at least under §102(e). EX1017, 1. Wyman discloses that when chips are stacked, shorter paths (e.g., 802) require less drive, while longer paths (e.g., 804) require a larger drive due to "increased resistance, capacitance and impedance," but it would be "wasteful" and "overkill" to use the "full capacity" of a driver for either path. EX1017, 1:22-24, 1:45-48, 6:15-50, Fig.8 (below); EX1003, ¶¶125-127.

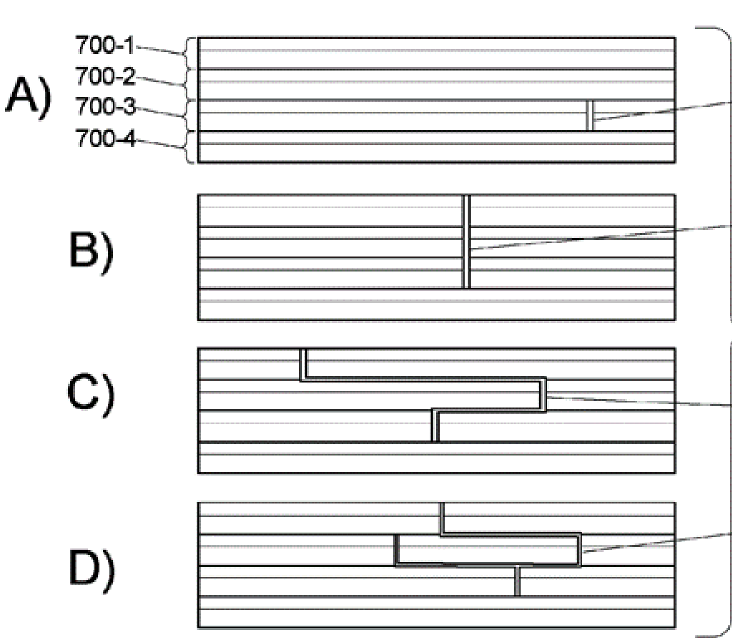


FIG. 8

E. Riho2 (EX1018)

U.S. Patent Publication No. 2010/0195364 ("Riho2"), published August 5, 2010, is prior art at least under §102(a). EX1018. Riho2 has the same inventor as Riho above, EX1016. Riho2 recognizes that the capacitive load will increase "as the number of stacked chips is increased," and thus discloses a circuit for

optimizing output drive capacity "according to a change in the time constant caused by parasitic capacitance and parasitic resistance." EX1018, ¶¶[0003, 0010, 0097], Fig.7A (below); EX1003, ¶¶128-130.

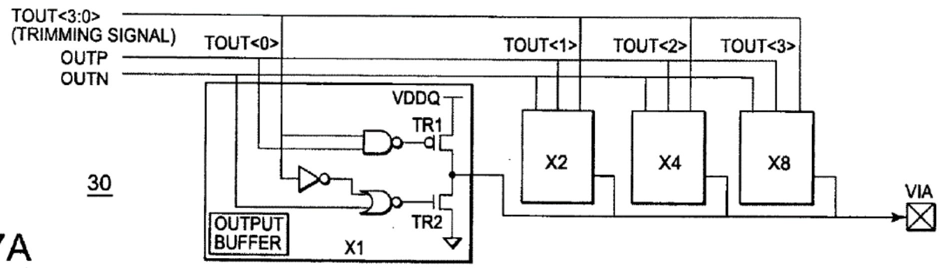


FIG. 7A

VI. CLAIM CONSTRUCTION

In related litigation, Patent Owner has interpreted some claim terms broadly for purposes of infringement, *see* EX1044, pp.63-68; EX1046, pp.63-69, even though a narrower interpretation may be more reasonable, but Petitioner contends that no express constructions are needed for this proceeding because the claims are obvious under either interpretation. EX1003, ¶112.

VII. ARGUMENT

A. Ground 1 (claims 1-20)

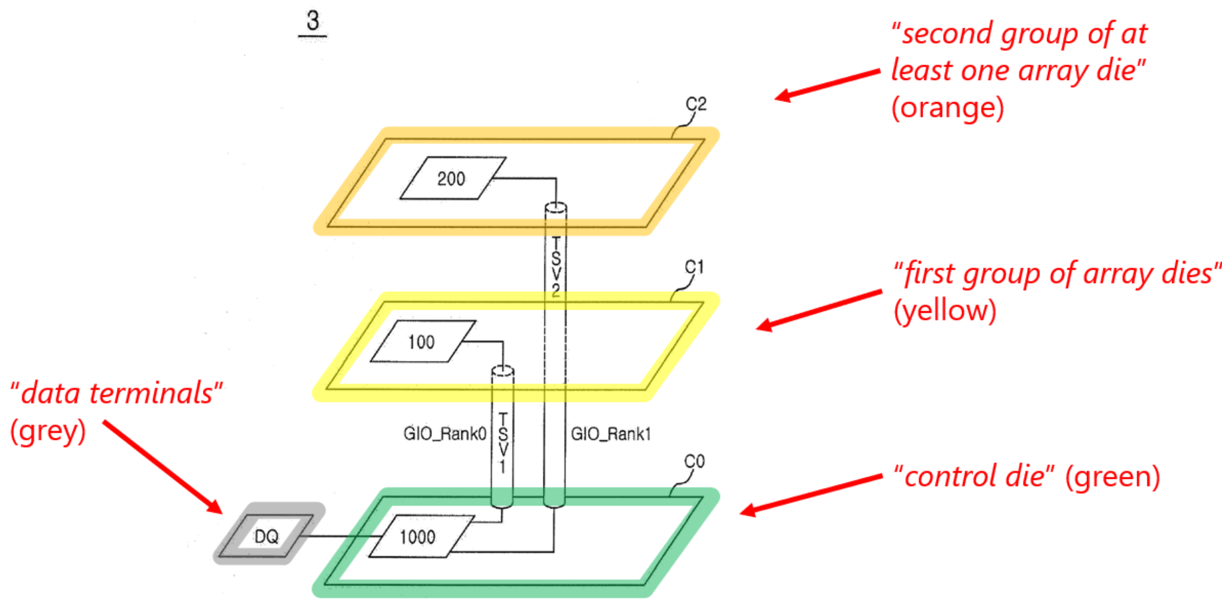
1. Ground 1 combination: Kim (EX1014) and Rajan (EX1015) and Wyman (EX1017)

Ground 1 first combines Kim (EX1014) with Rajan (EX1015), both of which, like the 160 Patent, disclose the same basic memory package structure including groups of stacked memory chips (yellow, orange) and a shared interface circuit (green). EX1014, ¶¶[0012, 50], Fig.5 (first below); EX1015, 1:51-60, 2:6-

7, 4:48-50, Fig.4 (second below); EX1001, 1:20-23, 5:26-29, Fig.2 (above p.14); EX1003, ¶¶146, 150-151.

Kim:

FIG.5



Rajan:

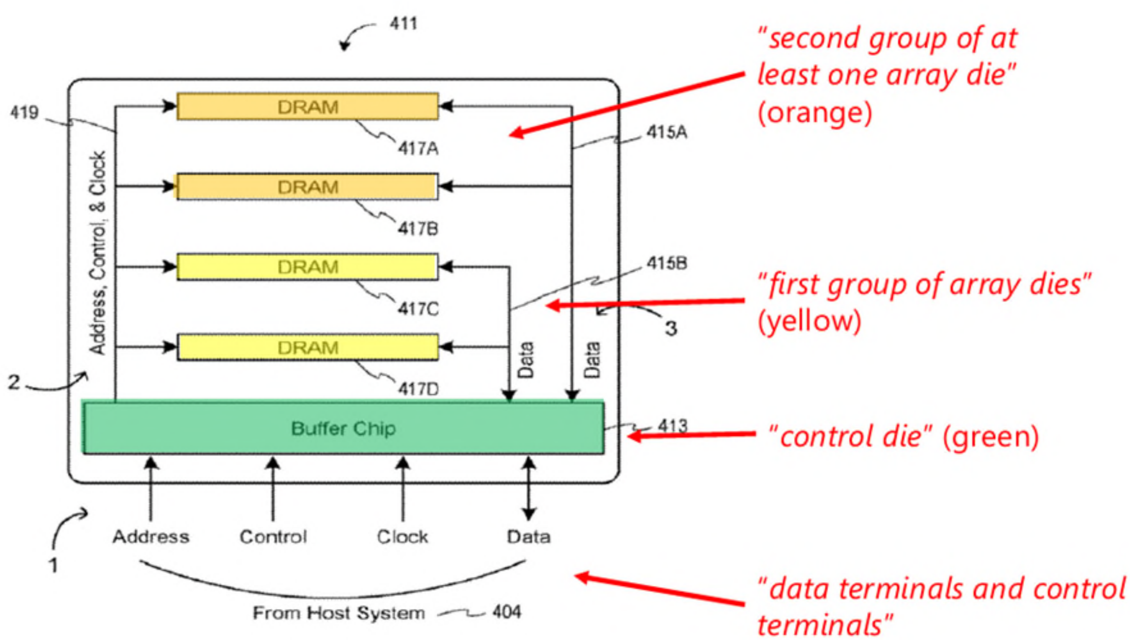


FIG. 4

A POSITA would have been motivated to combine Kim and Rajan for several reasons. First, as explained and shown above, they are analogous art with similar structures, so a POSITA would be motivated to look at the details taught by Rajan when implementing Kim, including details about the interface chip (green) and stacking the dies (yellow, orange). EX1003, ¶¶150-151.

Second, a POSITA would be motivated to create a package with an interface that complied with the well-known JEDEC standards, as taught by Rajan. EX1003, ¶¶148-149. Specifically, a POSITA would have found it obvious to use Rajan's terminals (e.g., in Figure 4, above) and corresponding data and control/address signals, in Kim's stacked memory package (e.g., in Figure 5, above) and been motivated to implement the functionality of a JEDEC compatible external data interface in Kim's control chip, as suggested by Rajan (including Figure 18, below), to make Kim's memory package compatible with the JEDEC standard. EX1014, ¶[0038], Fig.5; EX1015, 3:52-54, 8:8-11, Figs. 4, 18 (below); EX1003, ¶¶147-149. Indeed, the JEDEC standards were influential and well-known, as discussed above (p.5).

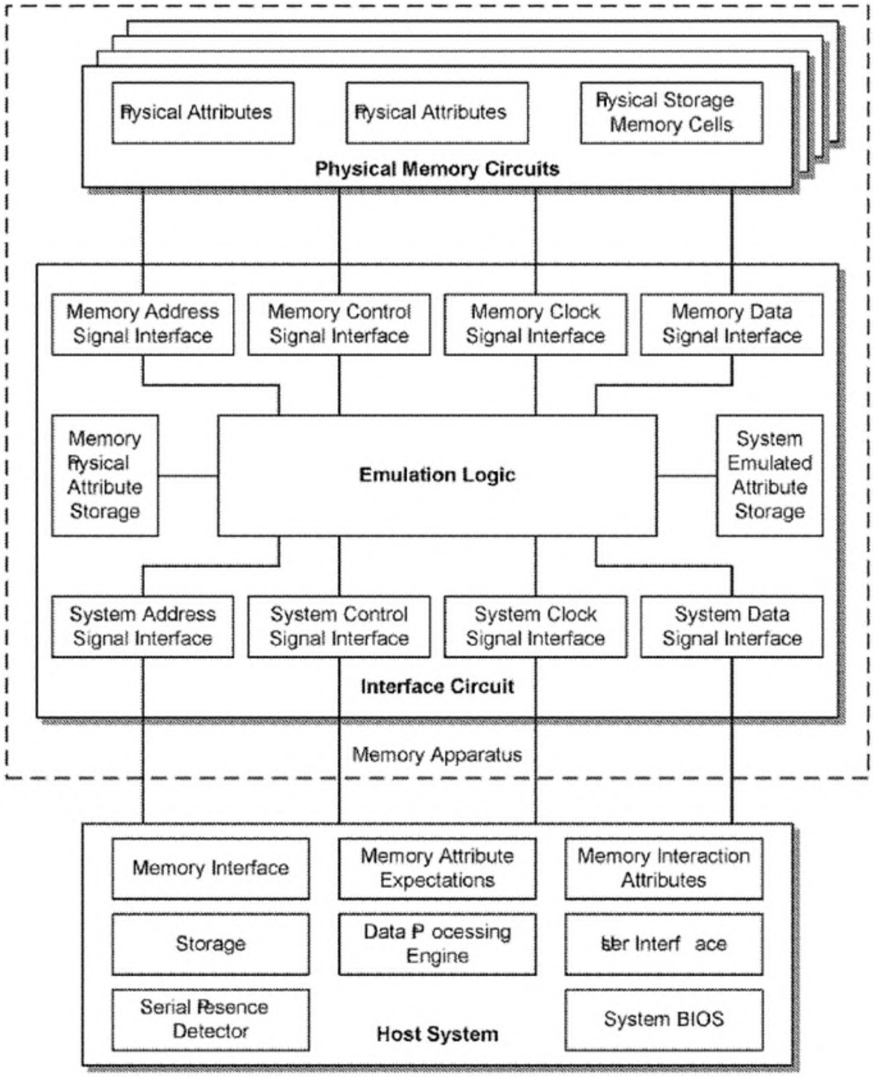


FIG. 18

Such a combination — following Rajan's suggestion to implement address, control, and data terminals following the JEDEC standards (including the DDR3 standard for stacked memory devices shown below, EX1019, p.12, Fig.3) — would have been well within a POSITA's level of skill since, as demonstrated by the 160 Patent's admitted prior art, emulating a standard JEDEC interface was a

known option (as discussed above, pp.8-11). EX1003, ¶¶151-153; EX1001, 22:22-24; EX1015, 5:36-43, 4:20-24, Fig.4.

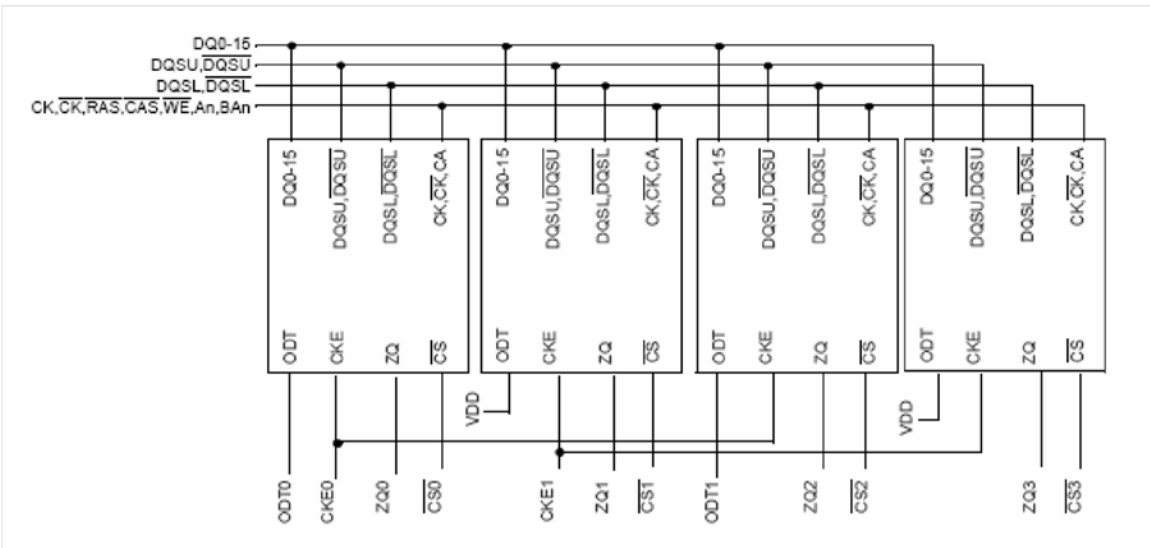
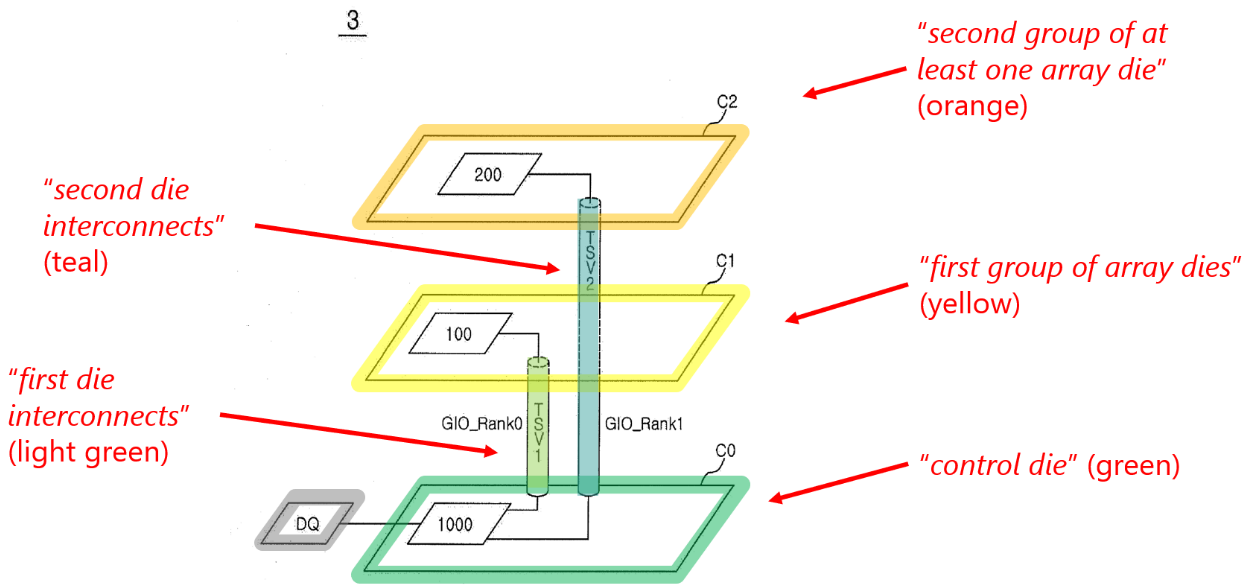


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

Third, a POSITA would have been motivated to look at Rajan for the details about adding more memory chips in the stack (resulting, e.g., in four chips, yellow and orange, in two groups, as shown below), as suggested by Kim's disclosure that "any number of … chips may be used." EX1003, ¶¶154-156; EX1014, ¶¶[0048, 50].

Kim:

FIG.5



Rajan:

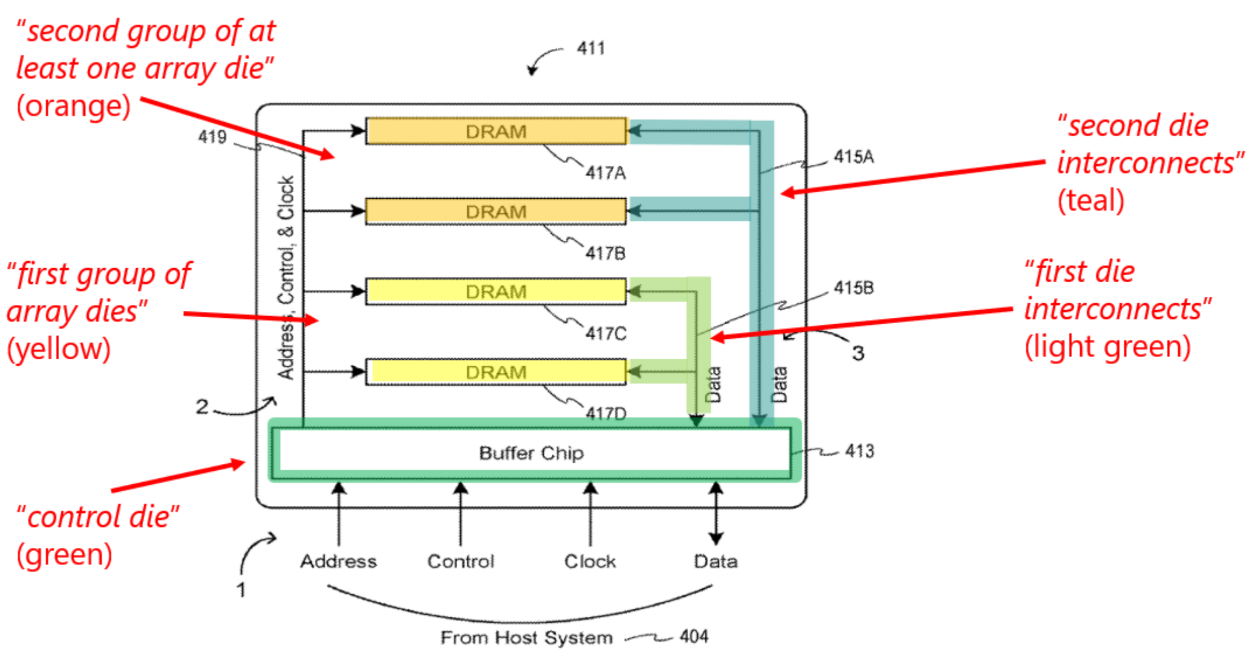


FIG. 4

A POSITA would have been motivated to implement a shared data bus for multiple memory chips as taught by Rajan (e.g., 415A and 415B, above) using, e.g., Kim's TSV interconnects (light green and teal, above), in part because a POSITA would have understood that there were a finite number of known ways to connect additional dies, including having a subset of dies sharing a through-silicon via (TSV). EX1003, ¶¶157-159; EX1015, 5:36-43, Figs. 2-6. Sharing a TSV among two or more dies was a known option, as confirmed by other references at the time (below). *See, e.g.*, EX1025, Fig.5 (below).

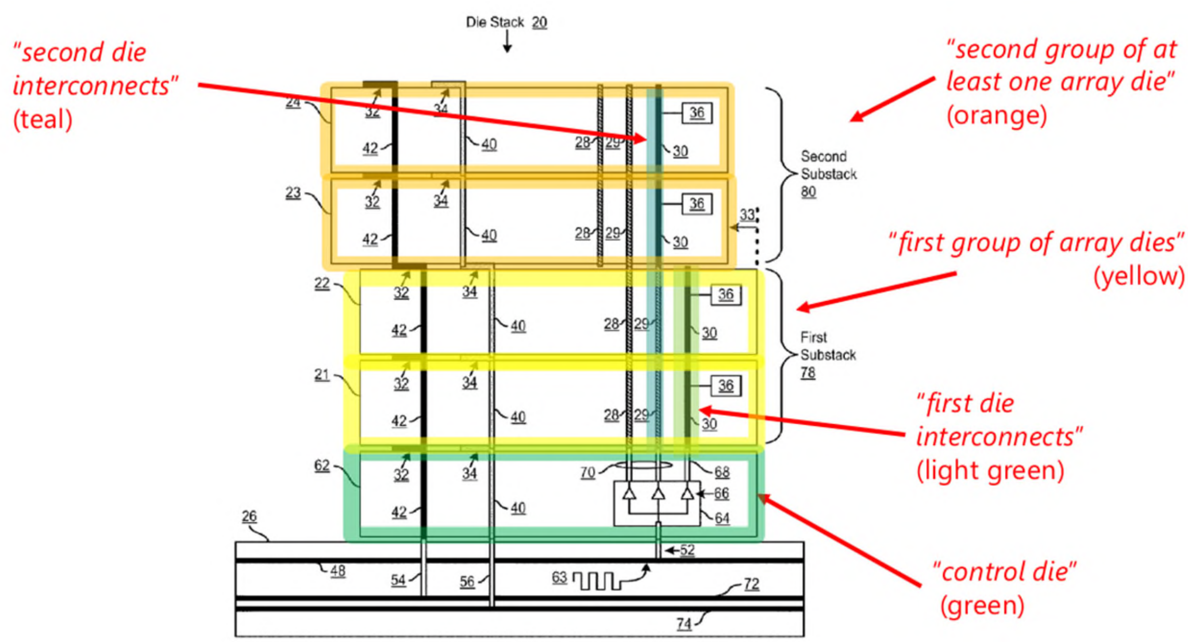


FIG. 5

Moreover, a POSITA would have been motivated to connect additional memory dies to Kim's TSV1 and TSV2 because it would not require creating new TSVs (which would add space and circuitry) and would allow emulating the JEDEC standard required by external devices. EX1003, ¶160; EX1015, 3:27-30, 3:52-61.

Furthermore, it was common at the time to have multiple memory dies sharing a single data bus. EX1003, ¶¶161-162. For example, when implementing "rank multiplication" (discussed above, pp.8-11), it was common to use a "fork-in-the-road" arrangement with two data buses for two ranks of memory devices (shown below left, yellow and orange), with the option of adding two additional ranks of memory devices (resulting in four ranks) to the existing data busses (shown below right, two yellow, two orange), meaning two memory dies (e.g., two orange) would share a given data bus. EX1003, ¶161; EX1026, Figs.12-13 (below); EX1027, pp.77-82 (Final Written Decision analyzing EX1026); *see also supra* pp.8-11; EX1001, 18:53-18:62, 19:26-32, 22:19-42.

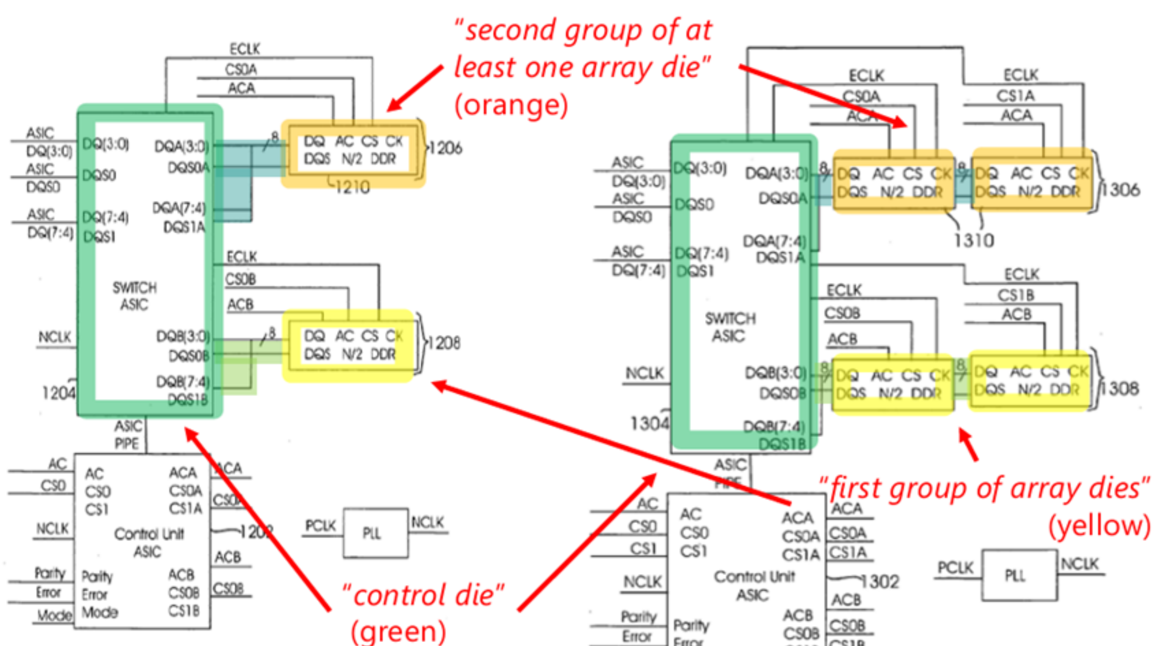


Fig. 12 Fig. 13

Figure 4 of Rajan teaches a similar arrangement as shown above (p.29), and a POSITA would have been motivated to implement that arrangement in Kim to preserve Kim's data collision avoidance feature without creating additional TSVs. EX1003, ¶163; EX1014, ¶¶[0042-44], Figs.4A-4B.

Ground 1 further combines Kim and Rajan with Wyman (EX1017). EX1003, ¶¶146, 165-171. Wyman is analogous art to Kim and the 160 Patent: its goal is to improve efficiency of signaling between stacked chips. EX1017, 1:45-48; EX1001, 1:21-23, 5:26-29; EX1014, ¶¶[0003, 0046]; EX1003, ¶¶168, 170. Wyman discloses that shorter paths (e.g., 802 below) have less load and thus require less drive, while longer paths (e.g., 804 below) have more load and thus require a larger drive, but it would be "wasteful" and "overkill" to use the "full capacity" of a driver for either path. EX1017, 1:22-24, 1:45-48, 6:15-50, 7:13-18, Fig.8 (below); *see also supra* pp.6-8 and EX1030, pp.135-138 (disclosing different-sized transistors to achieve different driver strengths).

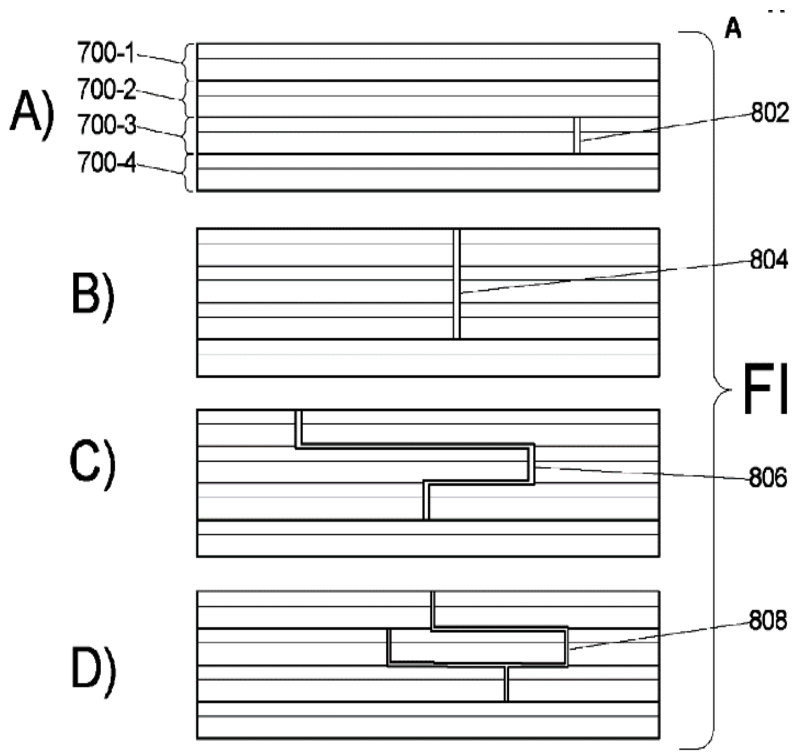
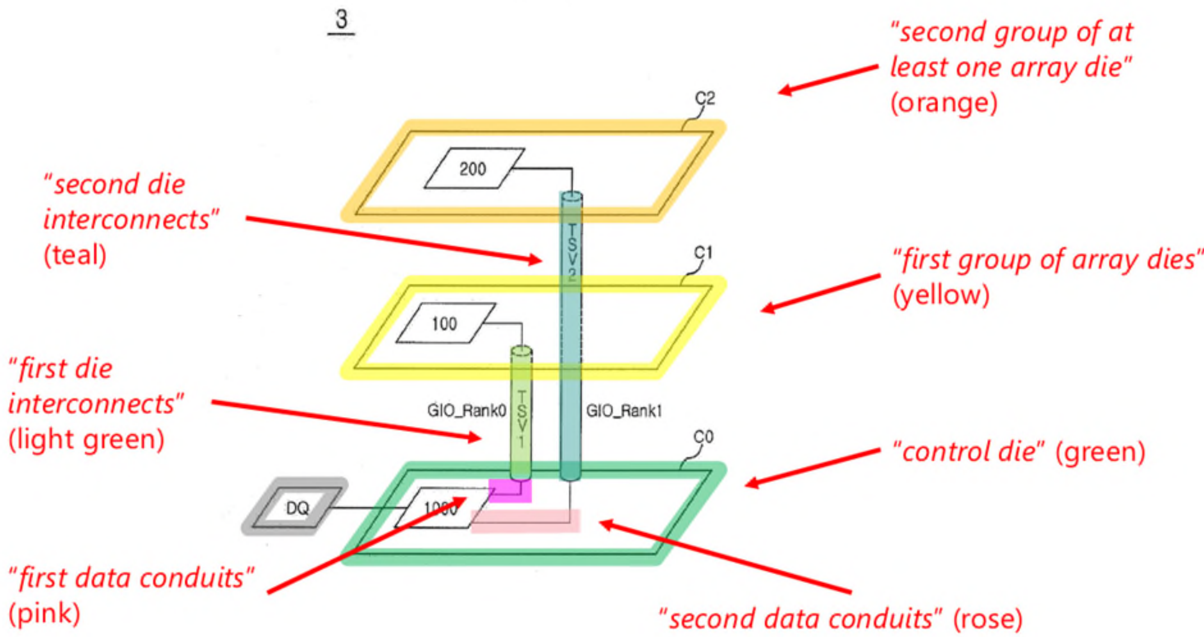
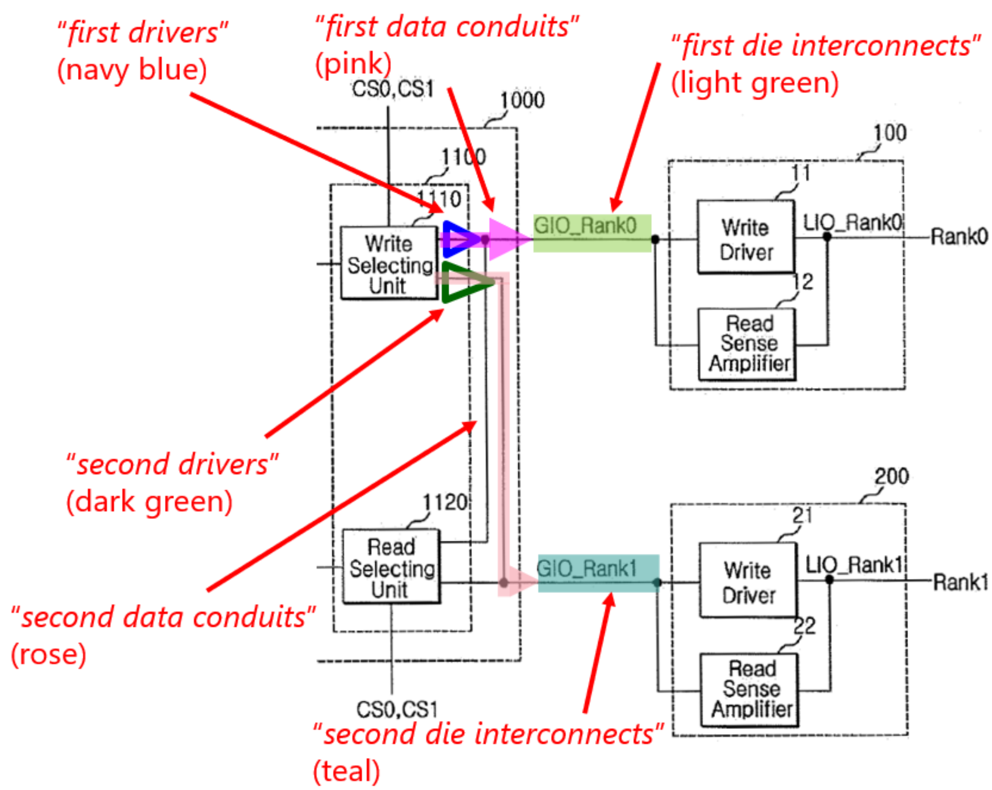


FIG. 8

A POSITA would have been motivated to implement Wyman's teachings in Kim to improve power efficiency by using smaller drivers (navy blue) for the shorter TSV1 (light green) and larger drivers (dark green) for the longer TSV2 (teal), as shown below, without using the full strength of a driver which Wyman teaches would be "wasteful and inefficient." *Id.*; EX1003, ¶¶167-170.

FIG.5


3
"second group of at least one array die" (orange)
C2
200
"second die interconnects" (teal)
TSV2
C1
"first group of array dies" (yellow)
100
"first die interconnects" (light green)
GIO_Rank0
TSV1
GIO_Rank1
C0
"control die" (green)
DQ
1000
"first data conduits" (pink)
"second data conduits" (rose)

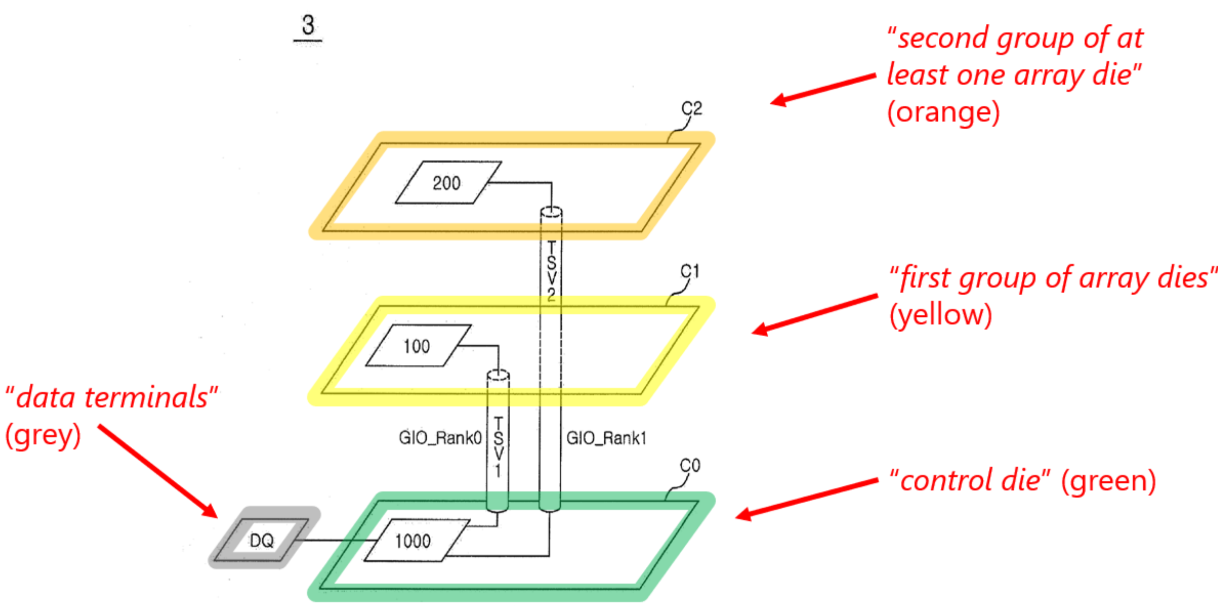

"first drivers" (navy blue)
"first data conduits" (pink)
"first die interconnects" (light green)
CS0,CS1
1000
100
1100
11
1110
Write Selecting Unit
GIO_Rank0
Write Driver
LIO_Rank0
Rank0
12
Read Sense Amplifier
"second drivers" (dark green)
200
1120
21
Read Selecting Unit
GIO_Rank1
Write Driver
LIO_Rank1
Rank1
"second data conduits" (rose)
22
Read Sense Amplifier
CS0,CS1
"second die interconnects" (teal)

2. Independent Claim 1

a) [1.a] Preamble

To the extent the preamble is limiting, Ground 1 teaches "*[a] memory package* [e.g., Kim's main chip C0 and stacked memory chips C1 and C2 in Figure 5 (below) which are "package[d] in a single package," EX1014, ¶¶[0046-47]], *comprising*." EX1003, ¶¶174-179.

FIG.5



b) [1.b] Data Terminals and Control Terminals

Grounds 1 teaches "*data terminals and control terminals*" via which the memory package communicates data [e.g., through Kim's data pad DQ (grey) in Figure 5 (below)] and control/address signals [e.g., read/write command signals including chip-select control signals CS0 and CS1 in Figure 2 (below) and address

signals A0-A15 per the JEDEC standard, e.g., EX1019, pp.6-13, 18, 33] with one or more external devices. EX1003, ¶¶180-196.

FIG.5

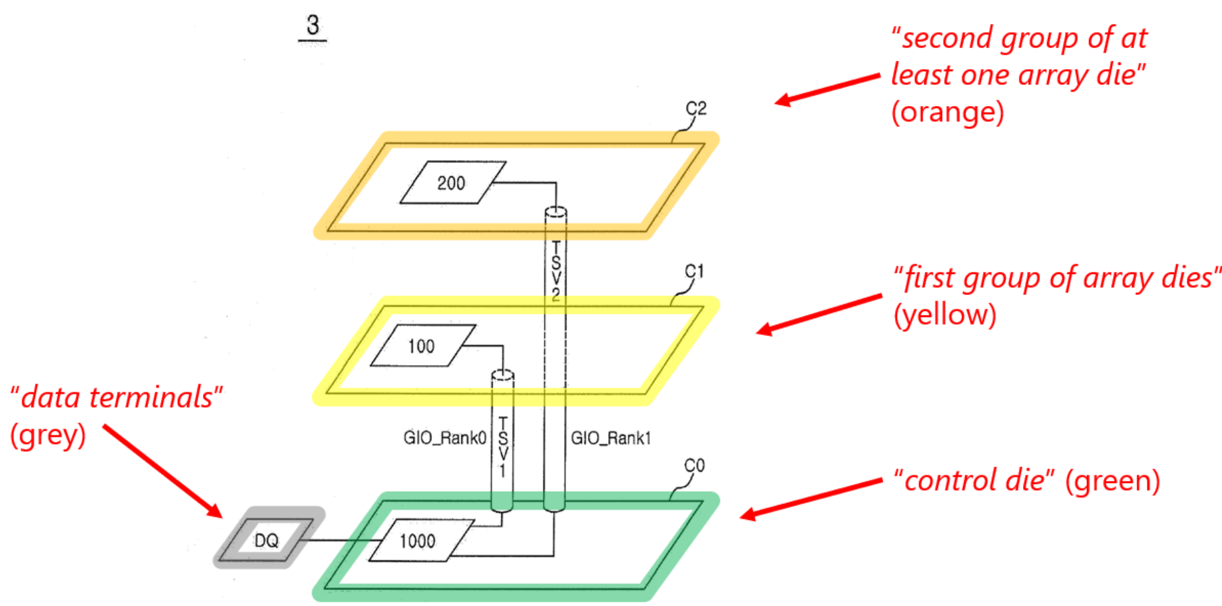
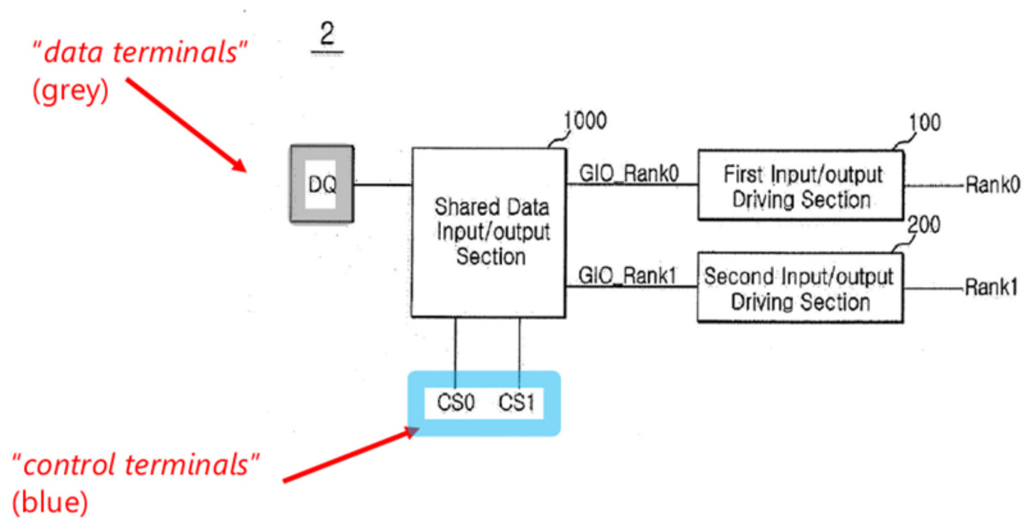


FIG.2



Kim describes the input/output section 1000 communicating data signals through a data pad "DQ" (grey above) during read and write operations. EX1014,

Abstract, ¶[0028]; EX1003, ¶¶183-184. A POSITA would have understood that data pad "DQ" is one of multiple "*data terminals*." EX1019, pp.3-12 (describing x4, x8, and x16 memory devices having 4, 8, and 16 DQ data terminals to communicate data with external devices); EX1003, ¶185.

In Ground 1 (pp.23-32), it would be obvious for Kim's signals to comply with JEDEC. Thus, Kim's chip selection signals CS0 and CS1 would be control signals that are part of the command signals that control the memory devices. EX1014, ¶¶[0006, 0032], Fig.2 (above); EX1019, p.13 (chip select signals are "considered part of the command code"); EX1003, ¶¶186-187. Under the JEDEC standards for stacked memory devices, and as admitted by the 160 Patent, chip-select signals are received from an external device at terminals on the memory package. *See, e.g.*, EX1019, pp.6-14 (describing pinout for stacked memories including terminals for data (DQ) and chip-select (CS) signals); EX1001, 1:32-58 (admitting prior art included memory packages with chip-select ports "configured to receive corresponding chip select signals to enable or select the array dies for data transfer"); EX1023, p.9, Fig.16; EX1022, pp.318-20, 332-35; EX1003, ¶188.

Under the JEDEC standards, Kim's "write and read command signals," EX1014, ¶[0038], would also include address signals received via terminals from an external controller. *See, e.g.*, EX1019, pp.6-14 (package pinout for stacked DDR3 memories including terminals for address signals A0-A15), p.18 (explaining

that read/write commands use row and column address signals), p.33 (Command Truth Table with Activate command with row address, and Read/Write command with column address); EX1001, 1:32-58 (admitting prior art included "command and/or address signals"); EX1003, ¶¶189-190.

Furthermore, a POSITA would have been motivated to implement Kim's control/address signals in light of Rajan (*see* pp.23-34), including Rajan's interfaces for sending/receiving address, control, and data signals to/from the host system in accordance with the JEDEC standards discussed above. EX1015, 2:6-7, 4:20-24, 5:36-43, 14:11-18, Figs.4 (below), 18 (interface circuit); EX1003, ¶¶193-194.

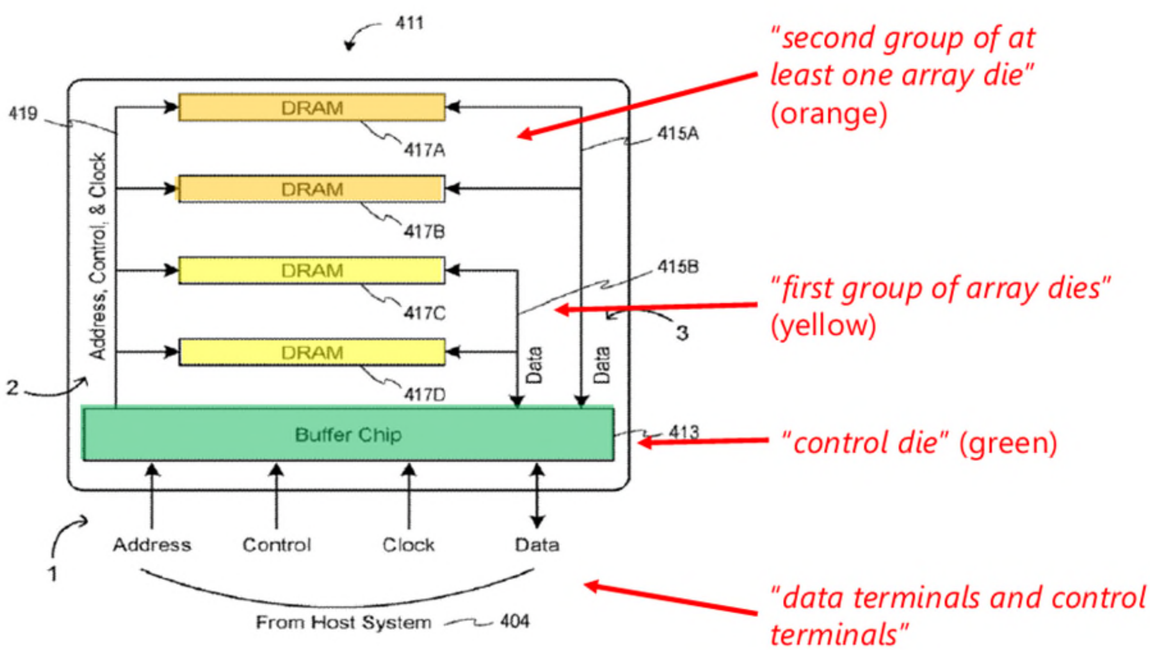
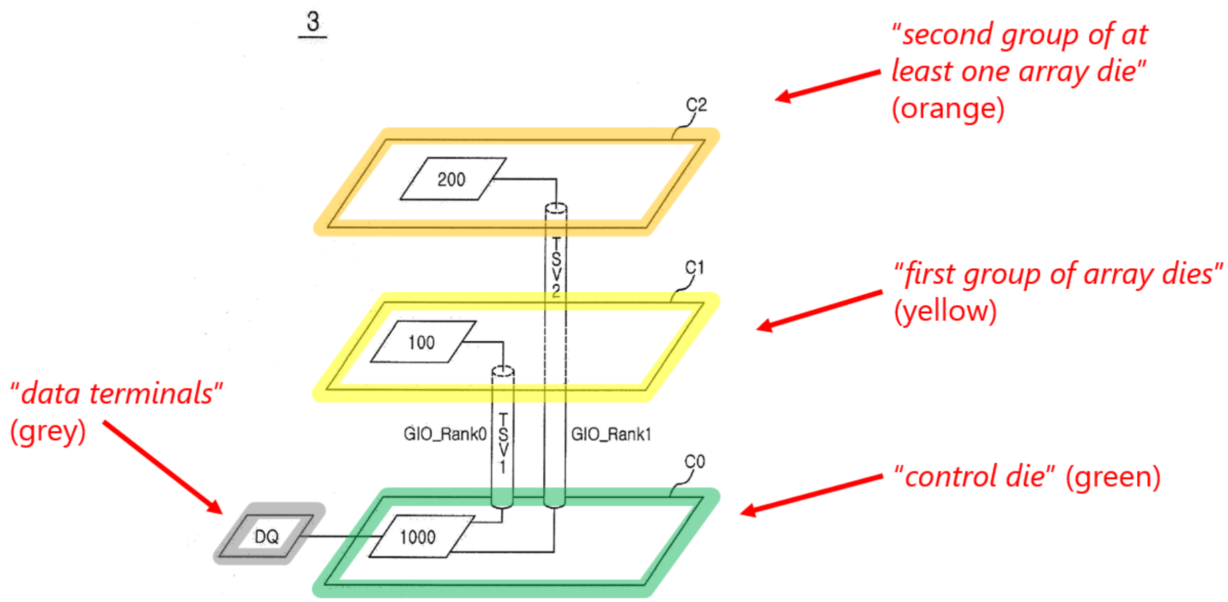


FIG. 4

c) [1.c] Stacked Array Dies

Ground 1 teaches "*stacked array dies including a first group of array dies* [e.g., including Kim's slave chip C1 (yellow), coupled to TSV1] *and a second group of at least one array die* [e.g., including Kim's slave chip C2 (orange), coupled to TSV2]." EX1014, ¶[0048] ("any number of … slave chips may be used"), Fig.5 (below); EX1003, ¶¶197-214.

FIG.5



A POSITA would have understood that Kim's "memory bank" for data storage in slave chips C1 and C2 would include a memory array (consistent with textbooks, below, and the JEDEC standards), rendering obvious the claimed "*array die[s]*." EX1014, ¶[0026] (describing using the input/output driving sections 100 and 200 to store data in respective memory banks); EX1019, p.13; EX1023, pp.1-2, Fig.2 (below); EX1022, pp.316-320 (same); EX1003, ¶¶201-202.

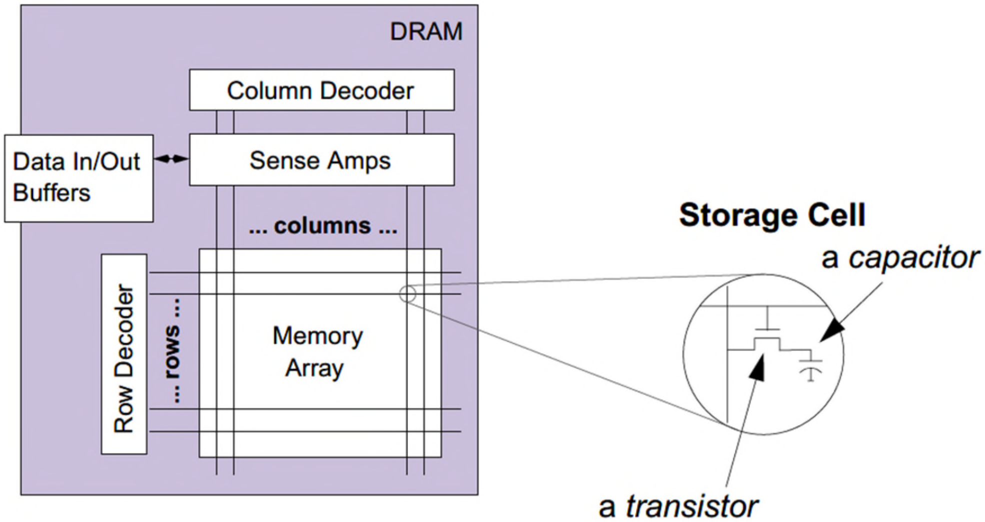
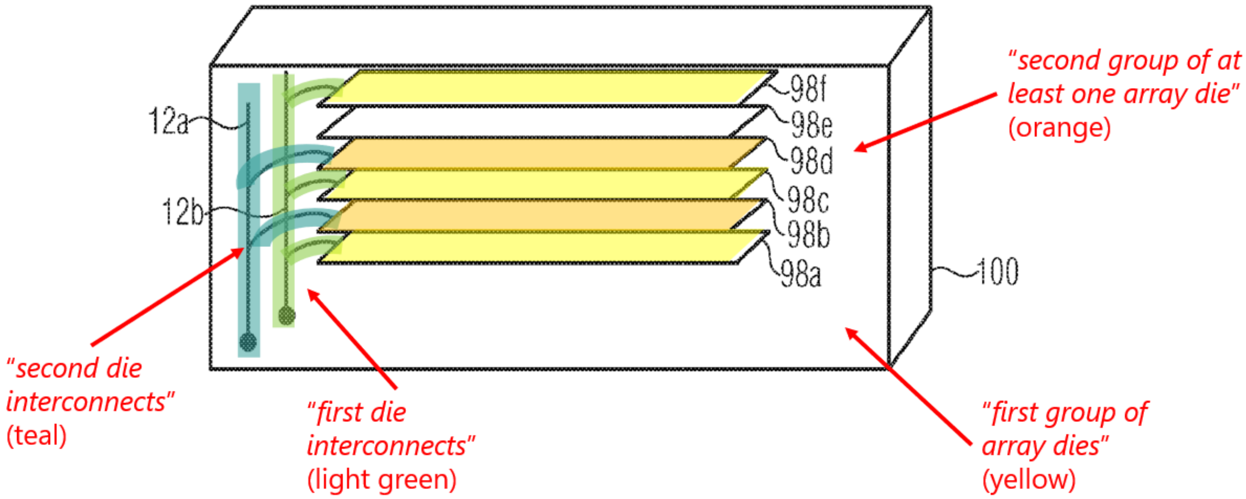


Figure 2: Basic Organization of DRAM Internals
The DRAM memory array is a grid of storage cells, where one bit of data is stored at each intersection of a *row* and a *column*.

Insofar as one might argue that "*first group of array dies*" requires multiple slave chips coupled to TSV1, Kim discloses that "any number of … slave chips may be used," EX1014, ¶¶[0048, 0050], consistent with other contemporaneous references (e.g., below) showing multiple groups of stacked dies, where each die in a group is connected to the same data interconnect, EX1024, 9:14-18, Fig.5 (below); EX1003, ¶¶204-205.



Additionally, Rajan discloses multiple stacked memory chips connected to the same data bus (below), thus further rendering obvious in the combination for Ground 1 that both the "*first*" and "*second*" "*group of array die[s]*" each include multiple "*array dies*" as explained in more detail above (pp.28-32). EX1003, ¶¶206-212.

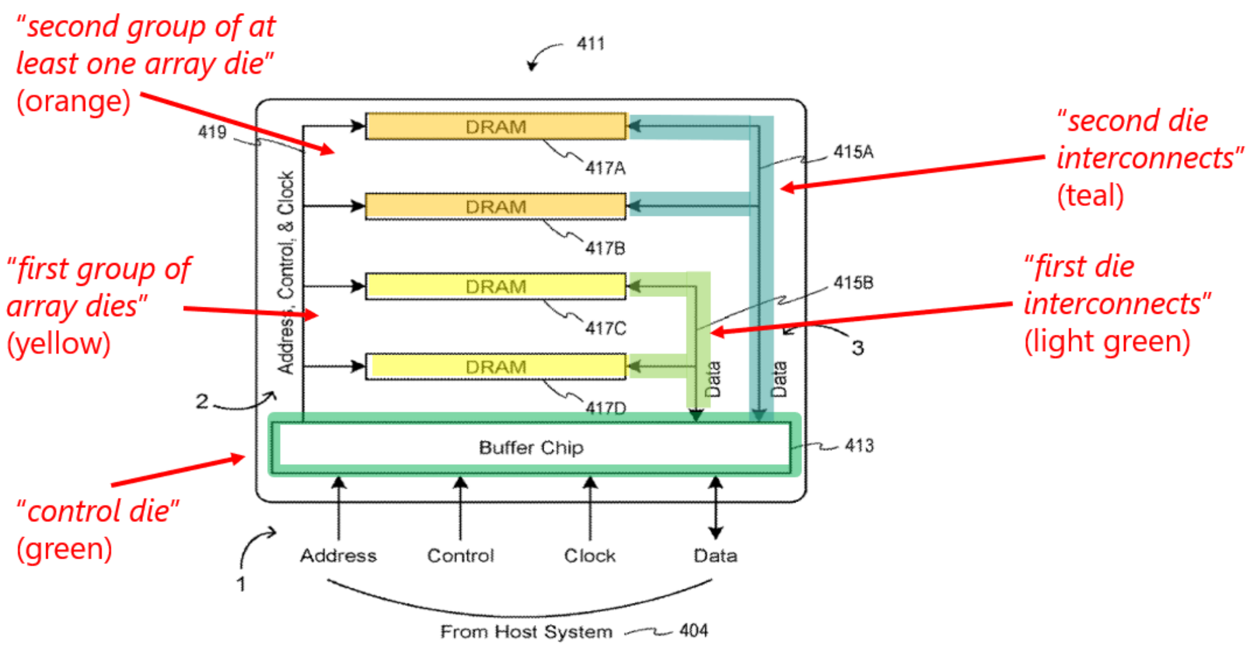


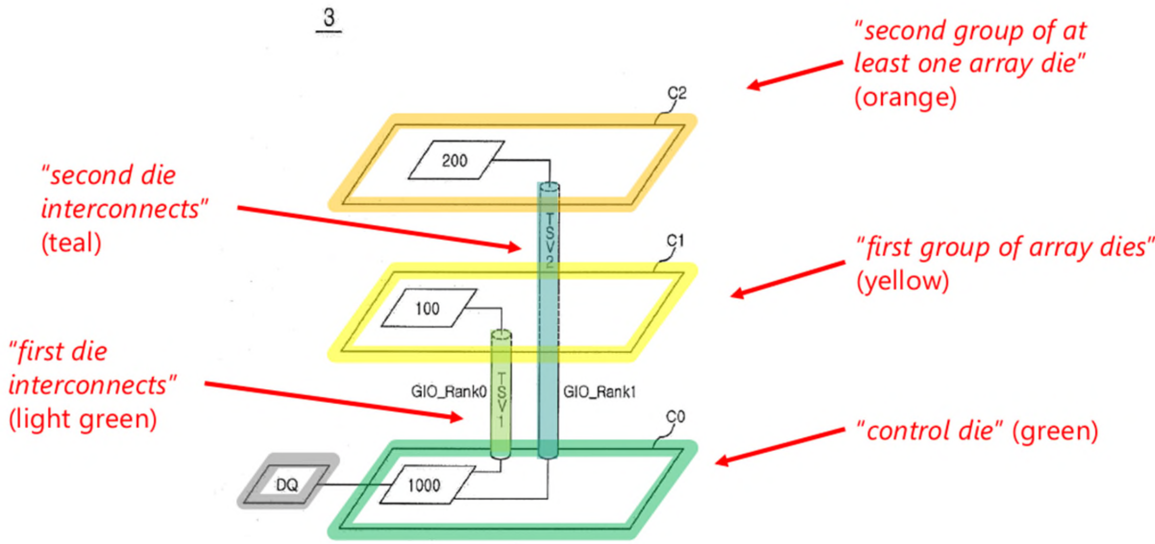
FIG. 4

d) [1.d.1]-[1.d.2] Die Interconnects in Electrical Communication with Array Dies

Ground 1 teaches "*first die interconnects* [e.g., Kim's through-silicon via TSV1] *and second die interconnects* [e.g., Kim's TSV2]*, the first die interconnects in electrical communication with the first group of array dies* [e.g., including Kim's slave chip C1] *and not in electrical communication with the second group of at least one array die* [e.g., including Kim's slave chip C2]*,*" and "*the second die interconnects* [TSV2] *in electrical communication with the second group of at least one array die* [including C2] *and not in electrical communication with the first group of array dies* [including C1]." EX1014, ¶[0049], Fig.5 (below); EX1003, ¶¶215-225. As discussed for [1.b] (pp.35-37), each "*array die*" receives multiple data signals (e.g., 4, 8, 16, or more DQ signals), and each such data signal

can have its own TSV, *see, e.g.*, EX1016, ¶[0030]; EX1014, ¶[0028], resulting in multiple "*die interconnects*" to a given "*array die*." EX1003, ¶¶220.

FIG.5

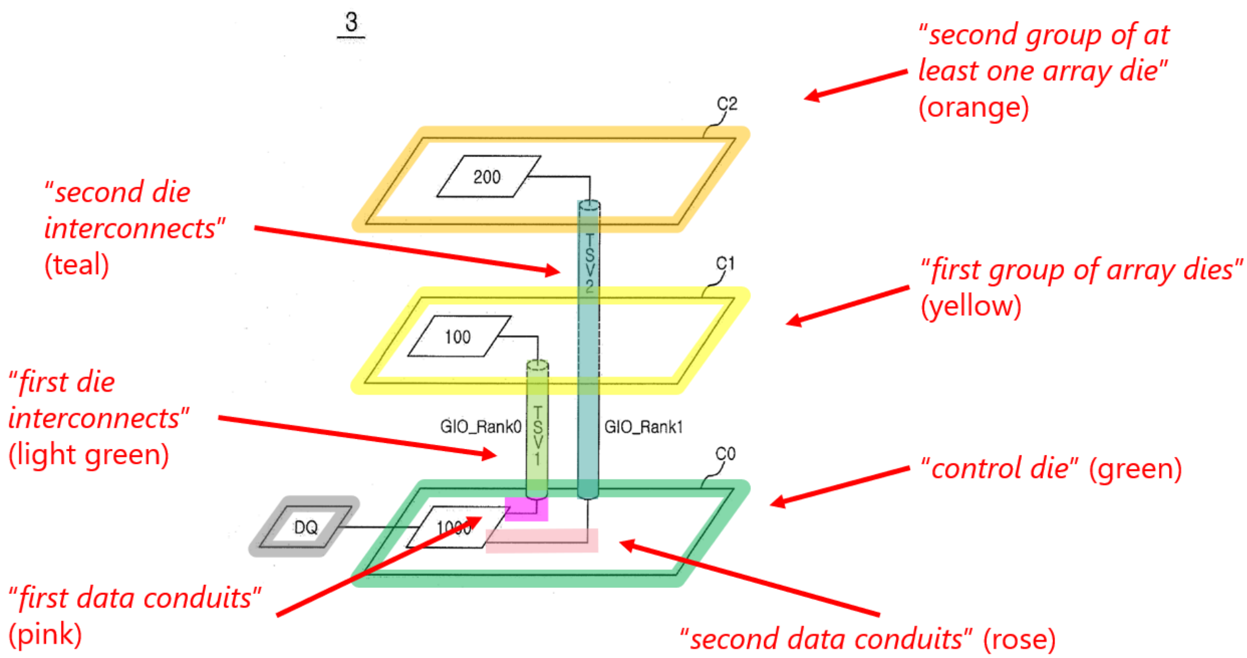


As shown above, the "*die interconnects*" labeled TSV1 do not extend up to C2 and thus are not "*in electrical communication*" with C2, while the "*die interconnects*" labeled TSV2 pass through C1 without being "*in electrical communication*" with C1 (e.g., TSV2 is not connected to input/output driving section 100 or anything else in C1). *Id.* Furthermore, a POSITA would have understood from Kim's disclosure that data collisions do not occur because, as illustrated in Figure 5, the data input/output lines through TSV1 and TSV2 are in electrical communication with one and not the other of chip C1 implementing Rank0, and C2 implementing Rank1. EX1014, Abstract, ¶[0045]; EX1003, ¶¶218-219, 223.

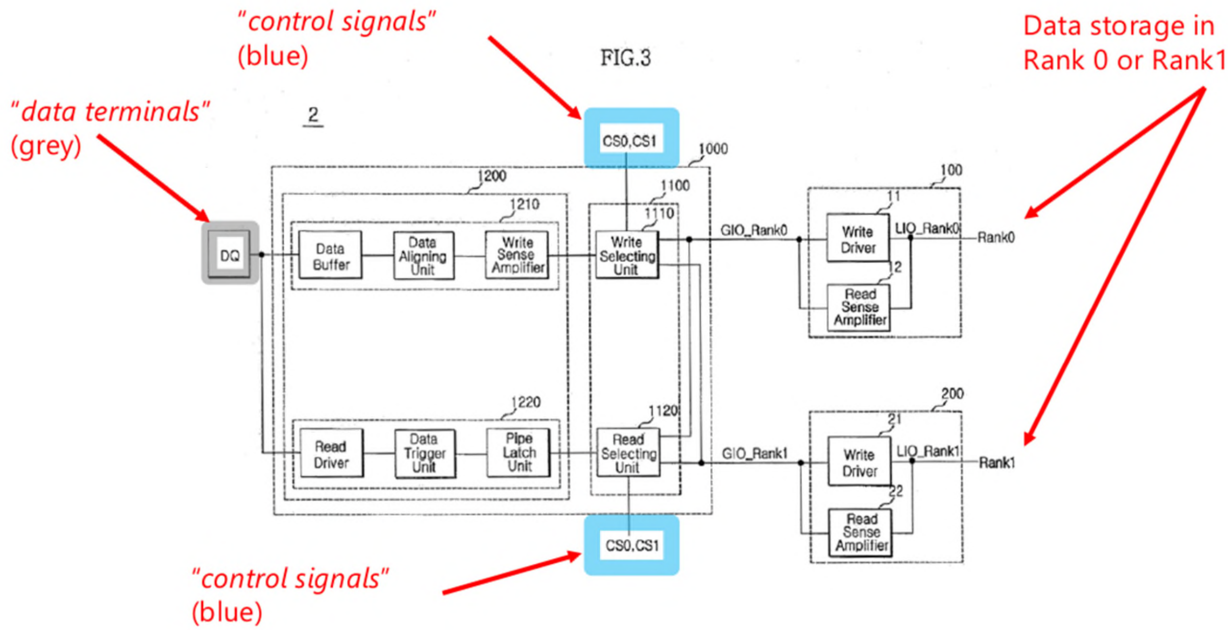
e) [1.e.1] Control Die

Ground 1 teaches "*a control die* [e.g., including Kim's main chip C0 (green)] *comprising*." EX1014, ¶¶[0038, 45], Figs. 3, 5 (below); EX1003, ¶¶226-234.

FIG.5



Kim teaches that the main chip C0 ("*control die*") controls the operation of the memory apparatus, including read/write operations in response to their respective commands from an external device, and that rank selecting unit 1100 (below) in the "*control die*" distinguishes these operations for the first rank (in the "*first group of array dies*") and the second rank (in the "*second group of … array die[s]*"). EX1014, ¶¶[0038, 45], Fig.3 (below); EX1003, ¶¶229-231.

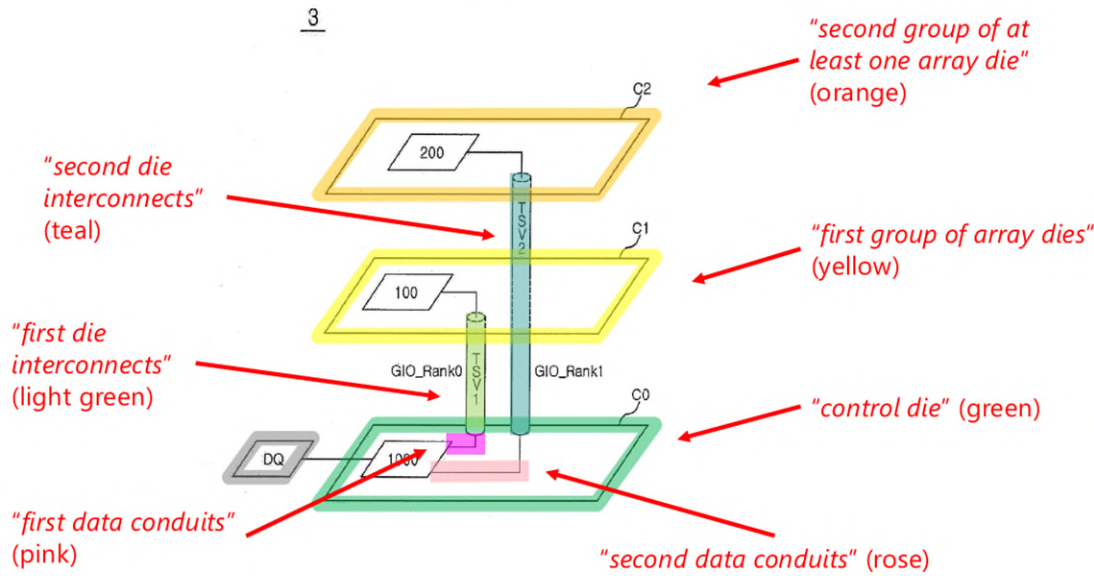


Moreover, the Kim-Rajan combination for Ground 1 (*see* pp.23-34) teaches that the "*control die*" can emulate one or more characteristics (e.g., using rank multiplication, *see* pp.8-11) different from those of the physical memory devices. EX1003, ¶232; EX1015, 6:30-7:67, Fig.18.

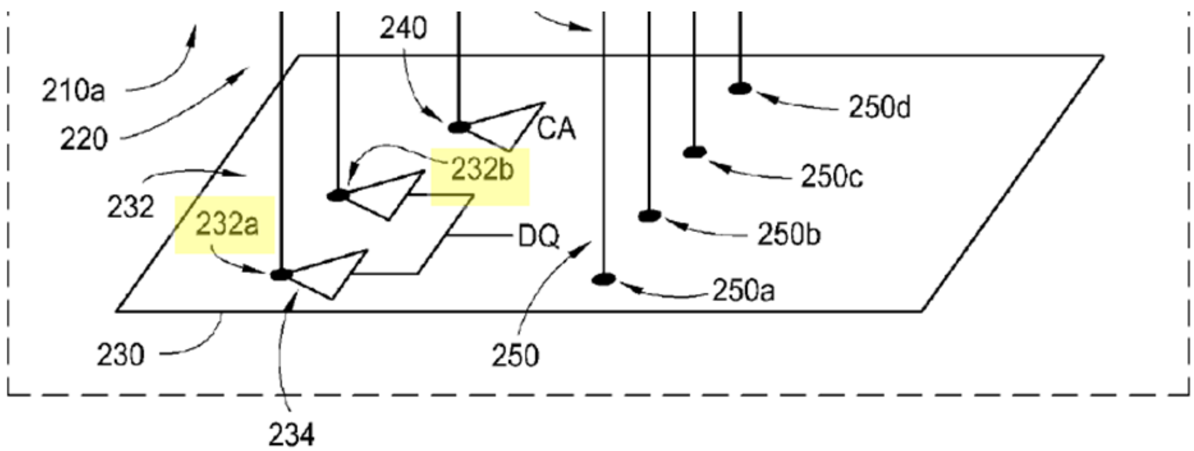
f) [1.e.2]-[1.e.3] First and Second Data Conduits

Kim's Figure 5 (below) shows that Ground 1 teaches "*first data conduits* [including signal lines (pink) for communicating data through data input/output section 1000] *between the first die interconnects* [such as TSV1 (light green)] *and the data terminals* [e.g., data pad DQ (grey)], *and second data conduits* [including signal lines (rose) for communicating data through data input/output section 1000] *between the second die interconnects* [such as TSV2 (teal)] *and the data terminals* [e.g., data pad DQ (grey)]." EX1014, ¶[0049], Fig.5 (below); EX1003, ¶¶235-251.

FIG.5

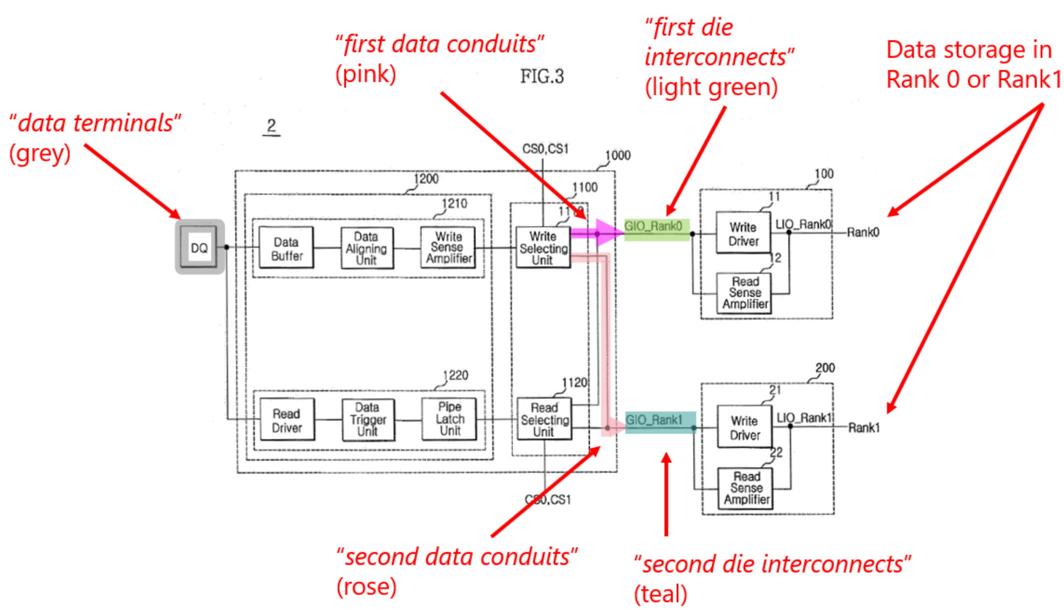


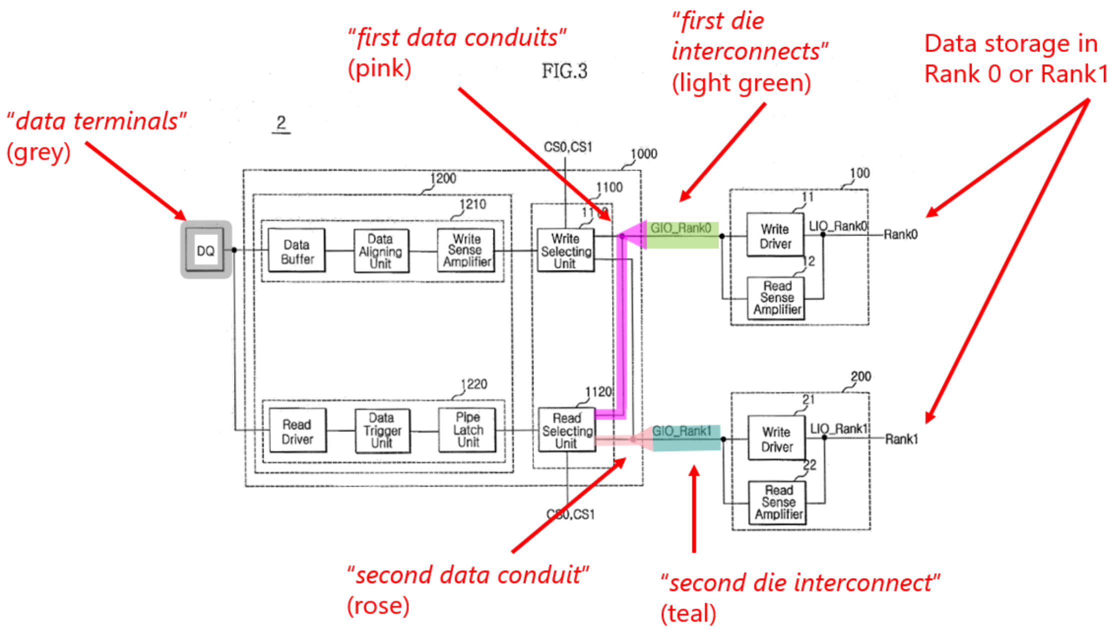
The "*data conduits*" in Kim (above) are similar to the "*data conduits*" 232a and 232b in the 160 Patent (below) that transmit data signals to respective die interconnects. EX1001, 6:51-65, 9:31-63, Fig.2 (below in part).



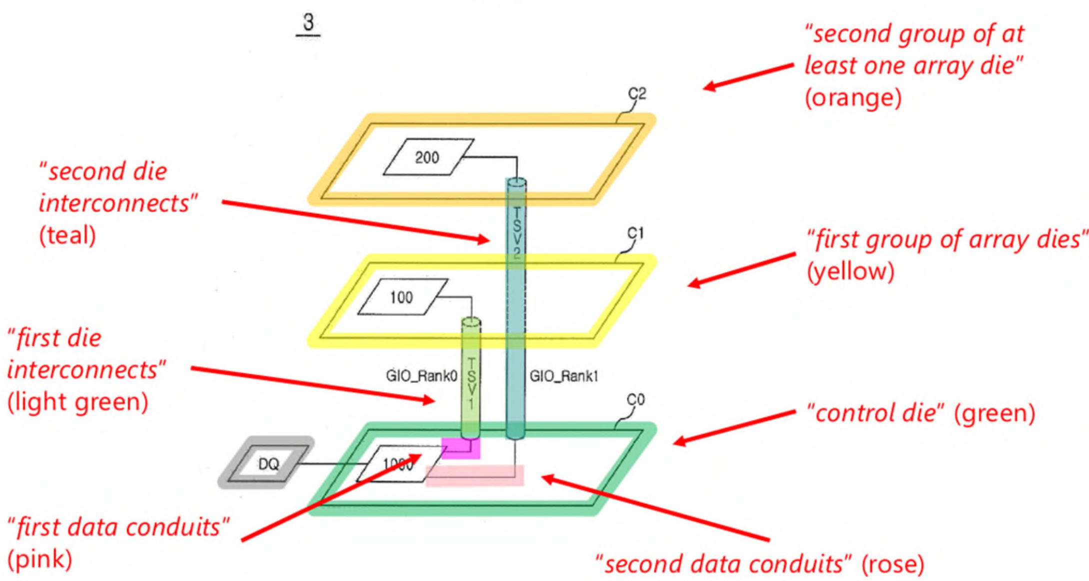
A POSITA would have understood from Kim's description of rank selection by chip selection signals (CS0, CS1) for read and write operations that the "*data conduits*" connecting the write selecting unit 1110 (below) and the read selecting

unit 1120 (below) in data input/output section 1000 (above and below) to TSVs in Rank0 are between "*the first die interconnects*," e.g., TSV1, and "*data terminals*," e.g., data pad DQ (grey, above and below), and the "*data conduits*" connecting the data input/output section 1000 (above and below) to TSVs in Rank1 are between "*the second die interconnects*," e.g., TSV2, and the "*data terminals*," e.g., data pad DQ (grey, above and below). EX1014, ¶¶[0029-30, 0035-38], Fig.3 (first below, showing first "*data conduits*" (pink) active for write operation to Rank0, or second "*data conduits*" (rose) active for a write operation to Rank1), and Fig.3 (second below, showing first "*data conduits*" (pink) active for a read operation from Rank0, or second "*data conduits*" (rose) active for a read operation from Rank1); EX1003, ¶¶239-248.





As explained above for claim limitation [1.b] (pp.35-37), Kim discloses that data pad DQ (grey) is one of the "*data terminals*" (e.g., for 4, 8, 16, or more DQ data signals). EX1003, ¶249. As further discussed above for limitations [1.d.1]-[1.d.2] (pp.42-43), it would be obvious that more than one data signal is communicated between the control die and an array die (like C1 or C2) by using multiple die interconnects for TSV1, and for TSV2, arranged as seen in Kim's Figure 5 (below), and that in such an arrangement, each die interconnect has a respective "*data conduit[]*" for transferring the corresponding data signal. EX1003, ¶237.



g) [1.e.4]-[1.e.5] First and Second Drivers

Ground 1 teaches "*the first data conduit[s]* [(pink)] *including first drivers* [(navy blue)] *each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*," and "*the second data conduit[s]* [(rose)] *including second drivers* [(dark green)] *each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size* [larger dark green triangle, given the longer TSV2] *being different from the first driver size* [smaller navy blue triangle, given the shorter TSV1]." EX1014, Figs. 3, 5 (below); EX1003, ¶¶252-266. The claim limitations "*the first data conduit*" and "*the second data conduit*" lack proper antecedent basis given that [1.e.2]-[1.e.3] recite "*first data conduit**s***" and "*second data conduit**s***."

EX1003, ¶253. Nevertheless, it would be obvious in light of Ground 1 that each "*data conduit*" could include one or more "*drivers*," as explained further below, thus rendering the claimed "*data conduit[s]*" obvious either way despite the lack of proper antecedent basis. *Id.*

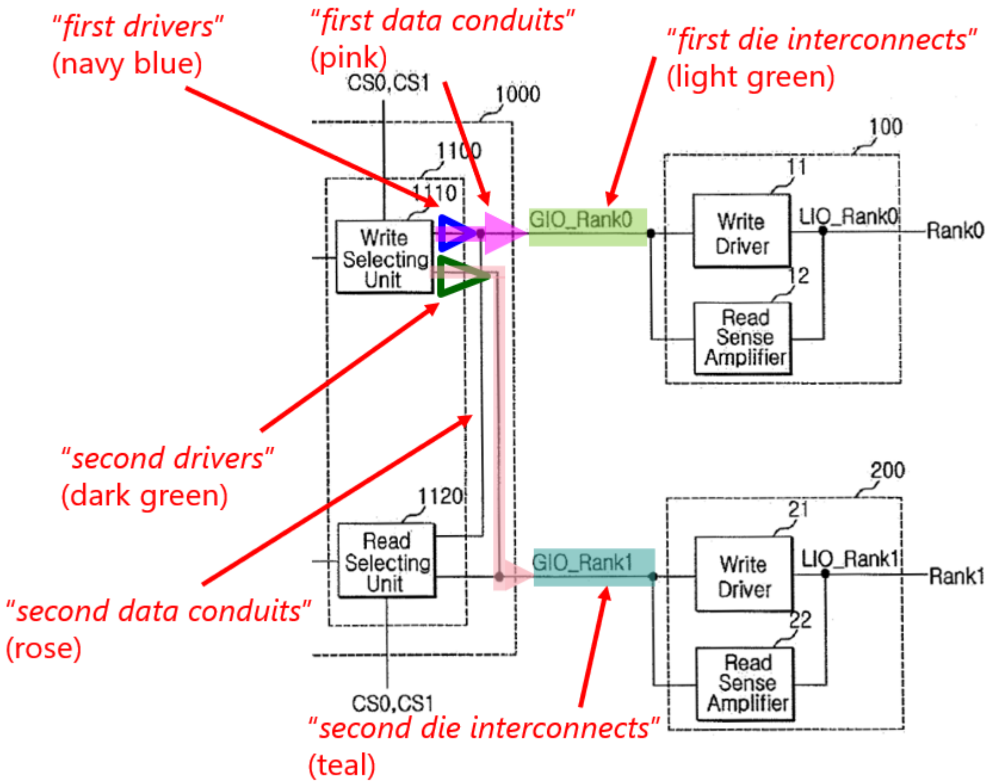
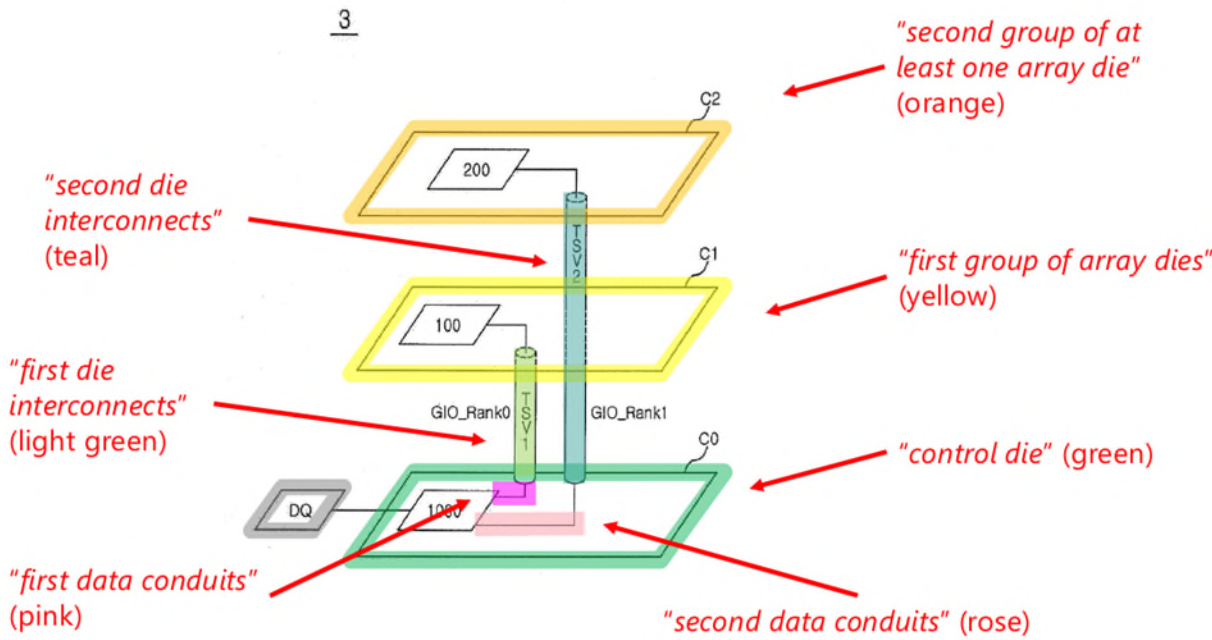


FIG.5



Given that Kim expressly illustrates in Figure 5 (above) that the first die interconnects, like TSV1, are shorter than the second die interconnects, like TSV2, a POSITA would have been motivated by Wyman (in the combination of Ground 1, pp.32-34) to use drivers of different strengths (i.e., "*first drivers*" having a "*first driver size*" and "*second drivers*" having a "*second driver size*") for Kim's different sized TSV1 and TSV2. EX1003, ¶¶257-265. As discussed above (pp.32-34), Wyman teaches that shorter paths (e.g., 802 below, like TSV1 above) have less load and thus require less drive, while longer paths (e.g., 804 below, like TSV2 above) have more load and thus require a larger drive, motivating a POSITA to drive the shorter TSV1 with a smaller drive, and the longer TSV2 with a larger drive, to use power in an efficient manner, but without using the full strength of a

driver, which Wyman teaches would be "wasteful and inefficient." EX1017, 1:22-24, 2:61-65, 6:15-30, 6:44-50, Figs. 7, 8 (below); EX1003, ¶¶257-265; *see also supra* pp.6-8 and EX1030, pp.135-138 (disclosing different-sized transistors to achieve different driver strengths).

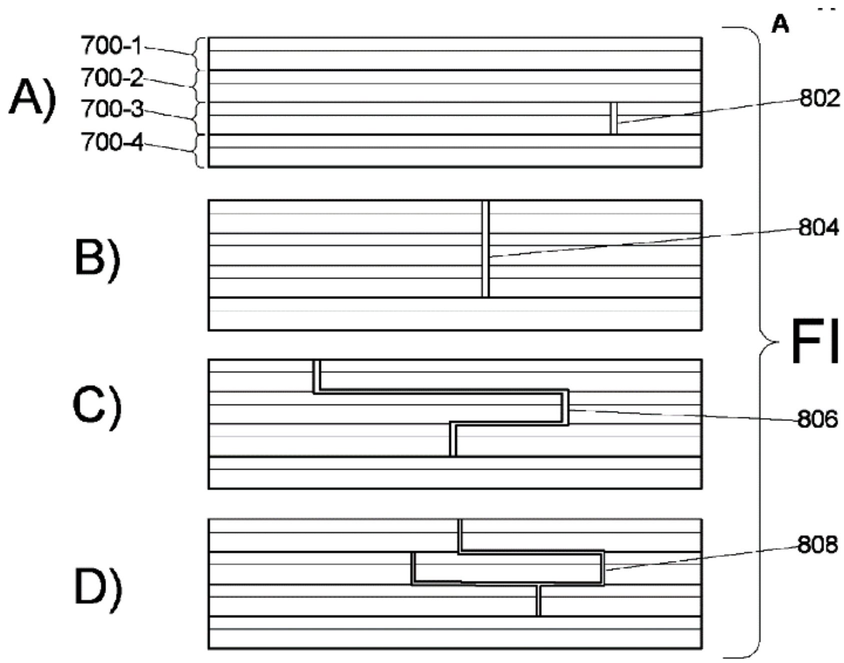
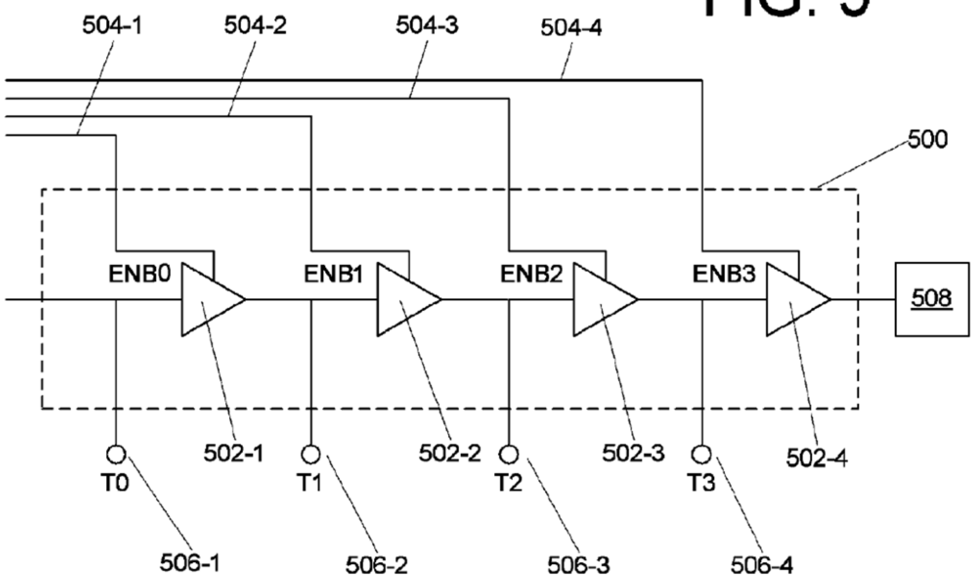


FIG. 8

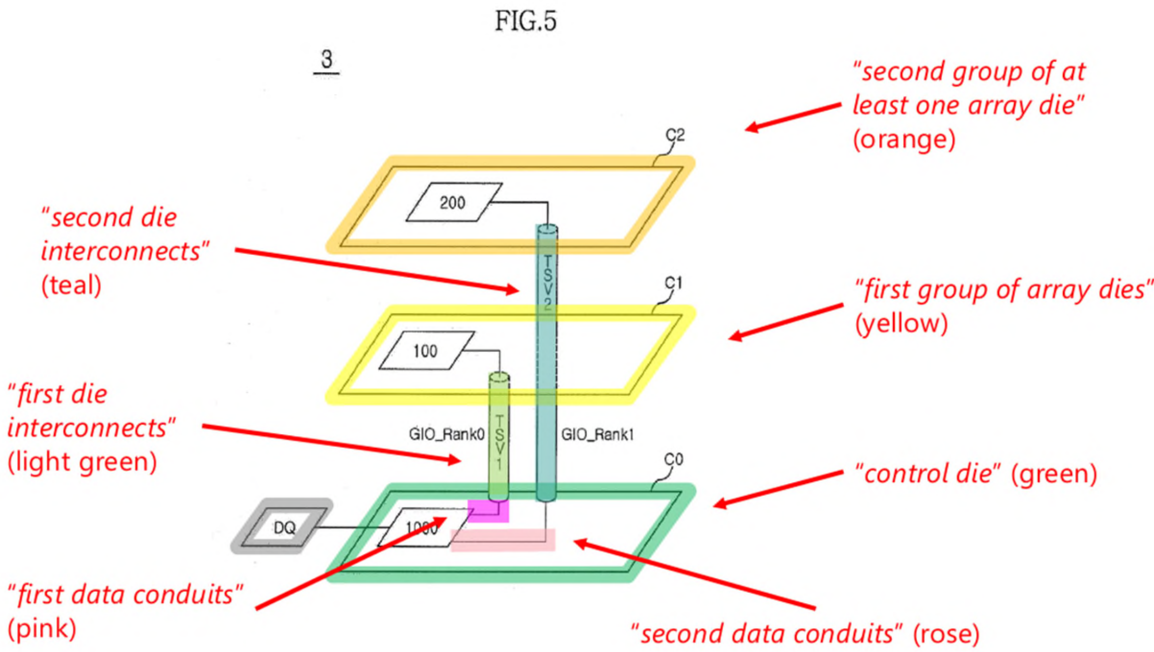
For example, Wyman discloses circuitry that includes one or more drivers (502-1 to 502-4, below) that are selectively activated to achieve the optimal driving strength for a given signal. EX1017, 5:11-14 ("a designer may now utilize and tap-off at five locations (506-1, 506-2, 506-3, 506-4, 508 [below]) depending on the drive requirements for a specific element or device"), 7:14-18 (describing modifying the output drive current to meet the requirements of a particular output load), Fig.5 (below), Figs.10-11; *see also supra* pp.6-8; EX1003, ¶260.

FIG. 5



3. <u>Claim 2</u>

Ground 1 teaches "*[t]he memory package of claim 1, wherein the second die interconnects* [from [1.d.2] (pp.42-43), e.g., TSV2 (teal, below)] *are longer than the first die interconnects* [from [1.d.1] (pp.42-43), e.g., TSV1 (light green, below)]*, and wherein the second driver size* [from [1.e.5] (pp.49-53)] *is larger than the first driver size* [from [1.e.4] (pp.49-53)]." EX1014, Fig.5 (below); EX1003, ¶¶267-272.



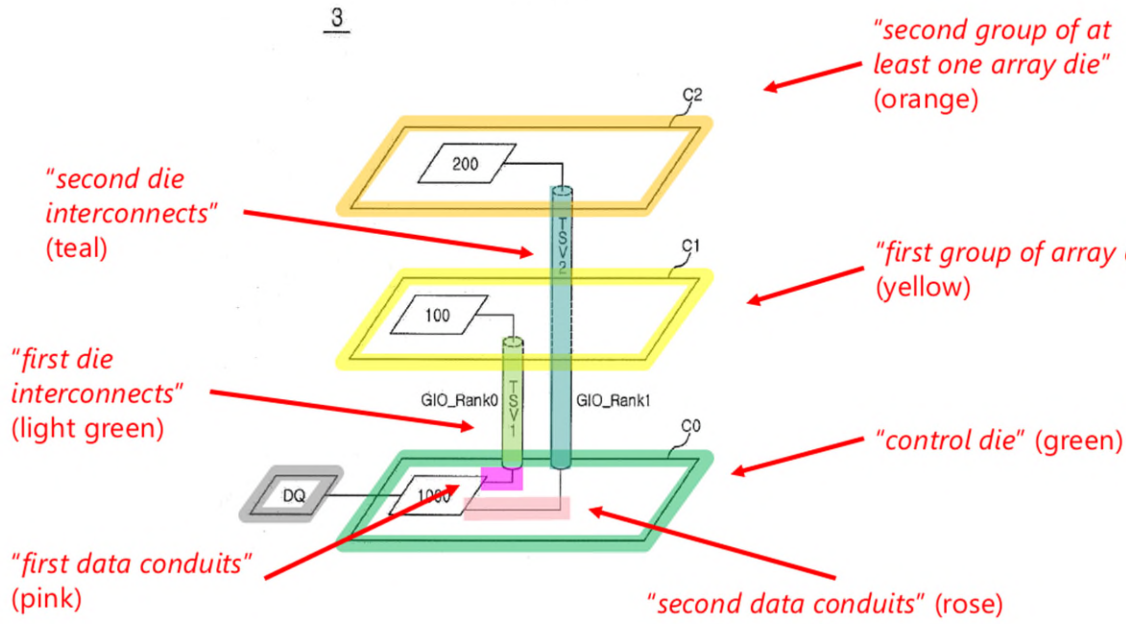
As discussed above for limitations [1.e.4]-[1.e.5], it would have been obvious to a POSITA that "*the second driver size is larger than the first driver size*" because Wyman teaches that the longer TSV2 of Kim is driven with a larger drive than the shorter TSV1. *Supra* pp.49-53; EX1003, ¶270.

4. Claim 3

a) [3.a] Second Die Interconnects are Longer than First Die Interconnects

Ground 1 teaches "*[t]he memory package of claim 1, wherein the second die interconnects* [from [1.d.2] (pp.42-43), e.g., TSV2 (teal, below)] *are longer than the first die interconnects* [from [1.d.1] (pp.42-43), e.g., TSV1 (light green, below)]." EX1014, Fig.5 (below); EX1003, ¶¶274-278.

FIG.5

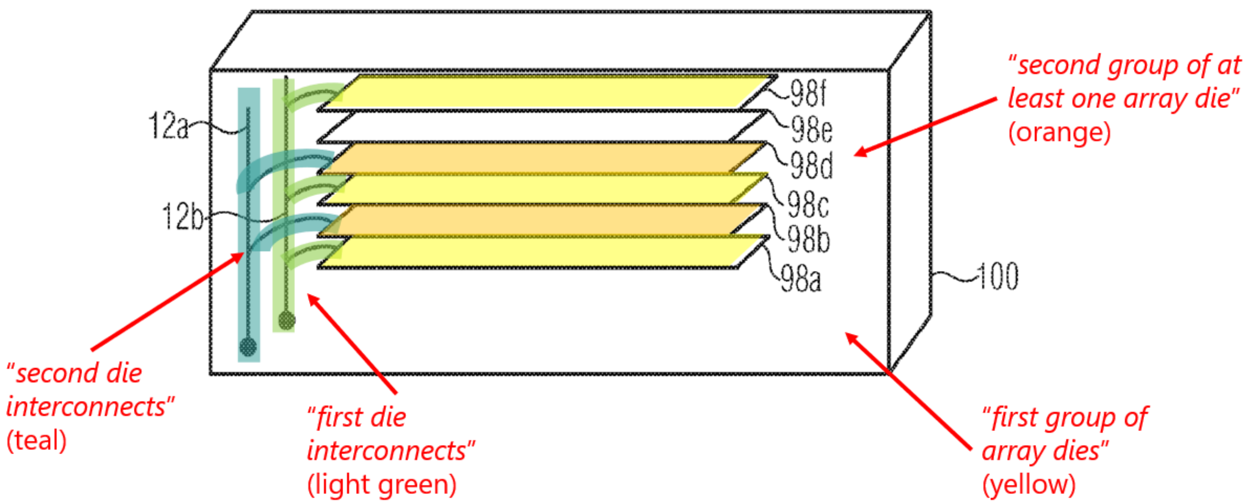


b) *[3.b] Number of Array Dies in the Second Group is Less Than Number of Array Dies in the First Group*

Ground 1 teaches "*wherein a number of array dies in the second group of at least one array die* [coupled to TSV2] *is less than a number of array dies in the first group of array dies* [coupled to TSV1]." EX1003, ¶¶279-290.

Kim teaches that "any number of main and slave chips may be used," EX1014, ¶¶[0048, 0050]; *see also id.* ¶[0027] ("one chip may operate as a plurality of ranks"), while Rajan teaches that the "memory circuits" in a stack of memory devices can either be "symmetrical" or "asymmetrical" (e.g., with memories of different capacities implementing one or more ranks), EX1015, 2:62-65, 7:63-67. Thus, in the combination of Kim and Rajan in Ground 1 (pp.23-32), it would be an obvious design choice to have an "asymmetrical" stack, resulting in fewer "*array*

dies in the second group" than "*in the first group of array dies*." EX1003, ¶¶282-285. Indeed, other contemporaneous references expressly disclosed such an arrangement (below), providing a further motivation for there to be fewer "*array dies in the second group*" than "*in the first group of array dies*." EX1024, 8:58-66, 9:14-18, Fig.5 (below); EX1003, ¶¶284-285.



Furthermore, as discussed above (pp.6-8, 32-34), a POSITA knew that the load on a given TSV increases with the length of the TSV and with the number of dies connected to the TSV, and that driving a signal on a TSV having a larger load requires a larger driver which uses more power. EX1017, 6:15-30, 7:14-26, Figs.7-8; EX1003, ¶¶286-287. Therefore, in an asymmetric arrangement where TSVs of different lengths are connected to different number of dies, a POSITA would have been motivated to arrange the stack so that a longer TSV (e.g., TSV2

in Kim) has fewer dies connected to it to reduce the power requirements of driving the longer TSV, as taught by Wyman. *See, e.g.*, EX1017, 2:61-65; EX1003, ¶288.

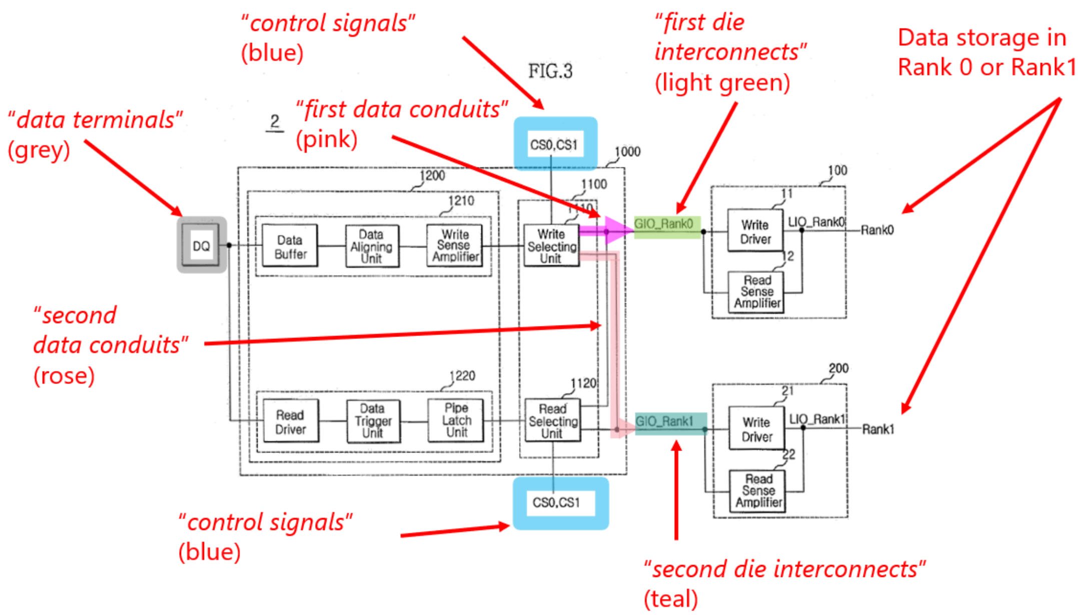
5. Claim 4

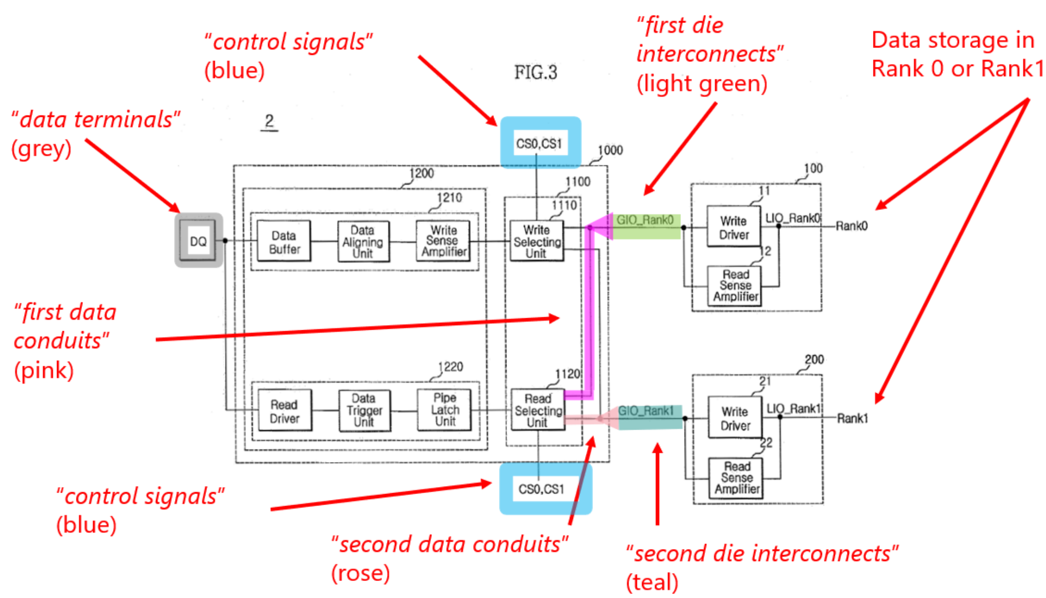
Ground 1 teaches "*[t]he memory package of claim 1, wherein the first driver size and the second driver size are related to a load on the first driver and a load on the second driver*," since a POSITA would have found it obvious, as explained for claim limitations [1.e.4]-[1.e.5], to follow Wyman's teaching of using different driver sizes corresponding to the different loads created by the TSVs of different lengths in Kim's stack. *See supra* pp.6-8, 49-53; EX1017, 7:14-26; EX1003, ¶¶291-297.

6. Claim 5

Kim's Figure 3 (below, annotated for write (upper) and read (lower) operations) shows that Ground 1 teaches "*[t]he memory package of claim 1, wherein the control die* [from [1.e.1], pp.44-45] *further comprises a control circuit* [e.g., in rank selecting unit 1100, including write selecting unit 1110 and read selecting unit 1120] *to control respective states* [e.g., to be active or not active, and if active to transmit data in the read direction or in the write direction] *of the first data conduits* [(pink) to TSV1] *and the second data conduits* [(rose) to TSV2] *in response to control signals* [including chip selection signals CS0 and CS1 and read/write command signals pursuant to the JEDEC standard, EX1019, pp.6-14,

18, 33; EX1023, p.9, Fig.16; EX1022, pp.318-20, 332-35] *received via the control terminals* [from an external device, as discussed for [1.b] (pp.35-38)]." EX1014, ¶¶[0032, 0035-36, 0038], Fig.3 (below); EX1003, ¶¶298-306.





7. **Claims 6-9**

The limitations of claims 6-9 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 1 for at least the same reasons discussed above:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[6.a]	[1.a]	¶¶308-311 (¶¶174-179)
[6.b]	[1.b]	¶¶312-315 (¶¶180-196)
[6.c]	[1.c]	¶¶316-318 (¶¶197-214)
[6.d.1]-[6.d.2]	[1.d.1]-[1.d.2]	¶¶319-321 (¶¶215-225)
[6.e]	[3.a]	¶¶322-324 (¶¶274-278)
[6.f]	[3.b]	¶¶325-327 (¶¶279-290)
[7.a]	[1.e.1]	¶¶329-332 (¶¶226-234)
[7.b.1]-[7.b.2]	[1.e.2]-[1.e.3]	¶¶333-336 (¶¶235-251)
[7.c.1]-[7.c.2]	[1.e.4]-[1.e.5][2]	¶¶337-339 (¶¶252-266)
[8]	[2]	¶¶340-344 (¶¶267-272)

[2] As explained above (pp.49-53), the singular "*first data conduit*" and "*second data conduit*" in [1.e.4]-[1.e.5] lack antecedent basis, but these limitations are obvious even if interpreted as plural "*first data conduit**s***" and plural "*second data conduit**s***" (like in [7.c.1]-[7.c.2]) as explained above (pp.49-53). EX1003, ¶339.

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[9][3]	[5]	¶¶345-351 (¶¶298-306)

8. <u>Independent Claim 10</u>

a) [10.a] Preamble

Ground 1 teaches "*[a] memory module* [e.g., <u>Kim</u>'s stacked memory devices implemented in <u>Rajan</u>'s memory module (below), which can be a JEDEC-standard DIMM format to be used in host systems with JEDEC-standard DIMM sockets] *operable in a computer system with a system memory controller* [e.g., the host system's JEDEC-compliant memory controller]*, comprising*." EX1015, 1:28-32 ("dual in-line memory modules (DIMMs)"), 3:5-7 ("memory controller (not shown)"), 8:52-54, 15:3-12, Fig.8 ("DIMM 800," first below); EX1014, ¶[0050]; EX1022, pp.316-20 (describing "memory controller" for JEDEC-compliant systems), Fig.7.2 (second below); EX1037, Fig.1, 1:34-39 ("Memory Controller Hub (MCH)"); EX1003, ¶¶353-362.

[3] In claim 9, "*the plurality of terminals*" lacks antecedent basis, but based on the surrounding claim language it appears that "*control terminals*" from [6.b] could be the claimed "*one or more second terminals of the plurality of terminals*," making the claim obvious like claim 5. EX1003, ¶¶348-350.

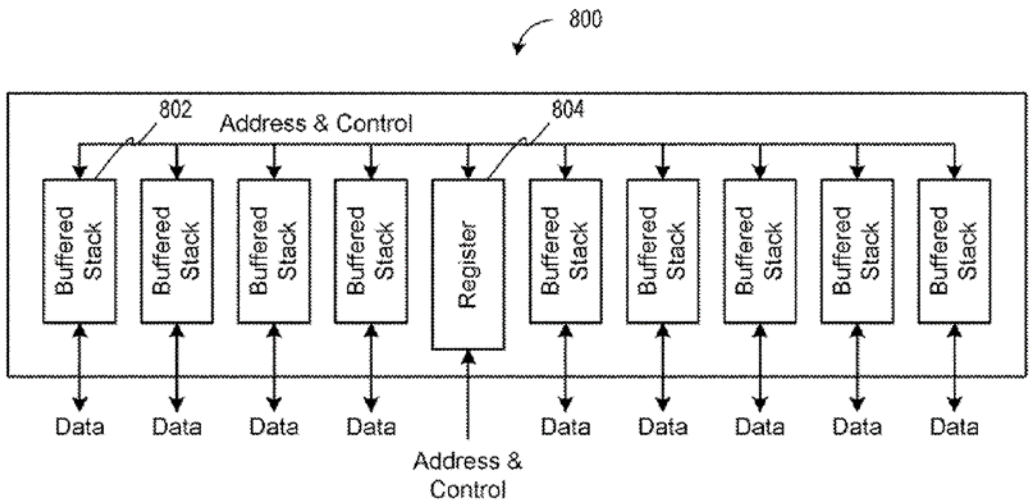


FIG. 8

316 Memory Systems: Cache, DRAM, Disk

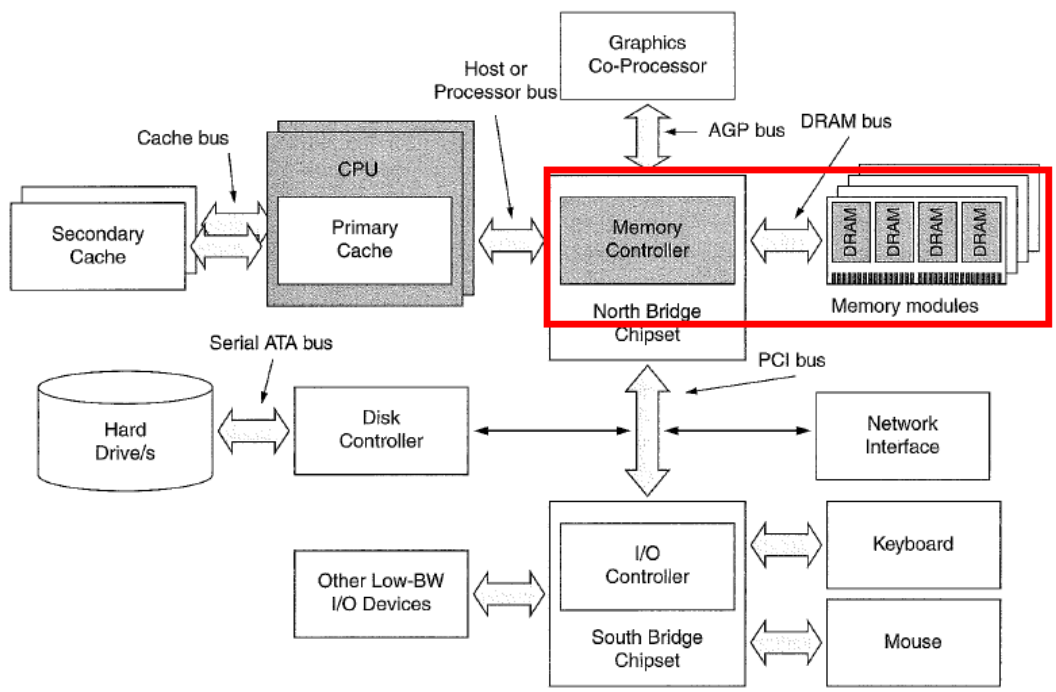


FIGURE 7.2: A typical PC organization. The DRAM subsystem is one part of a relatively complex whole. This figure illustrates a two-way multi-processor, with each processor having its own dedicated secondary cache. The parts most relevant to this report are shaded in darker grey: the CPU, the memory controller, and the individual DRAMs.

b) [10.b] A Register Device

Ground 1 teaches "*a register device* [e.g., Rajan's register 804, *see* EX1015, 8:52-58, Fig.8 (below)] *configured to receive input command/address signals* [*see id.* receiving "Address & Control" signals per the JEDEC standard, EX1015, 4:20-24, which would include command signals, *see* EX1019, pp.13, 33; EX1023, p.9, Fig.16; EX1022, pp.318-20] *from the system memory controller* [from [10.a] above] *and to output control signals* [e.g., Rajan's register outputting "Address & Control" signals (below), *see also* claim element [15.b] (pp.72-73)]." EX1003, ¶¶363-368; *see also* EX1022, pp.418-19 ("Registered Memory Module (RDIMM)").

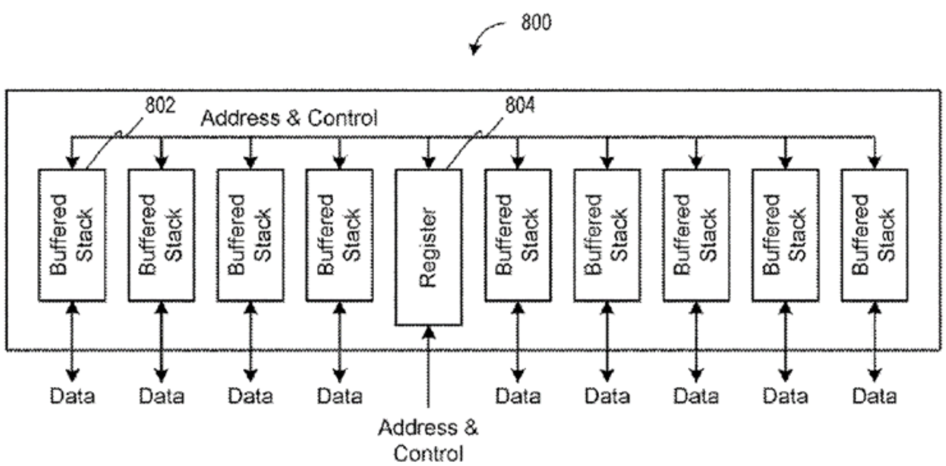


FIG. 8

c) [10.c] Plurality of DRAM Packages

Ground 1 teaches "*a plurality of DRAM packages* [e.g., buffered stacked DRAM circuits 802 (below)], *each DRAM package comprising*." EX1015, 8:52-58, Fig.8 (below); EX1022, pp.315, 374 (DRAM "packages"); EX1014, ¶¶[0046-47]; EX1003, ¶¶369-373.

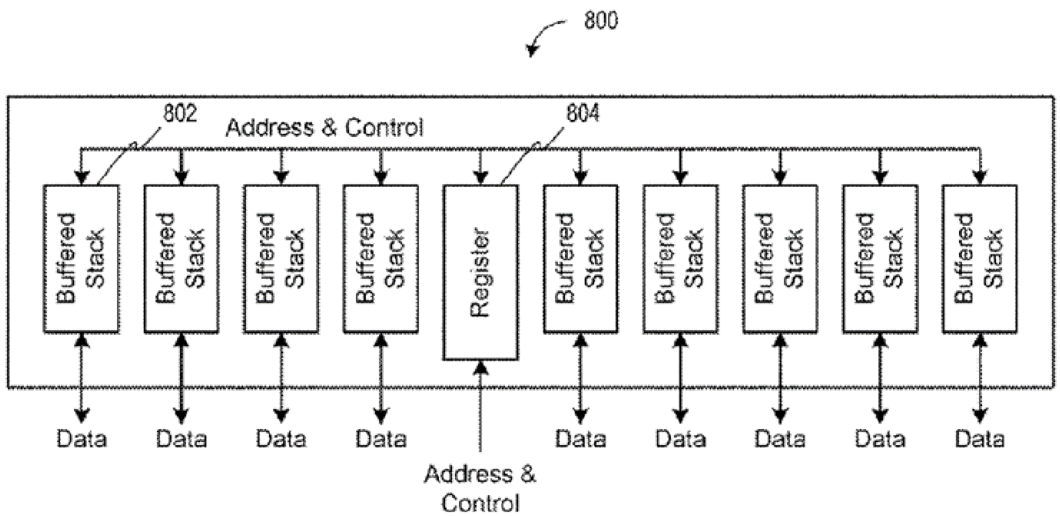


FIG. 8

d) [10.d] Data Terminals

Ground 1 teaches "*data terminals via which the DRAM package communicate data signals with the system memory controller* [as indicated below by "Data" with an arrow from the bottom of the DRAM package 802 to the system memory controller from [10.a] (pp.60-61), and as explained above for [1.b] (pp.35-38)], *and control terminals via which the DRAM package receive the control signals from the register device* [e.g., the "Address & Control" signals from the

Register 804 to the DRAM packages 802, as explained for [10.b] (p.62)]." EX1003, ¶¶374-379; *see also* EX1022, pp.418-19 ("Registered Memory Module (RDIMM)"); EX1019, pp.6-13 (JEDEC standard for terminals for data, address, and control).

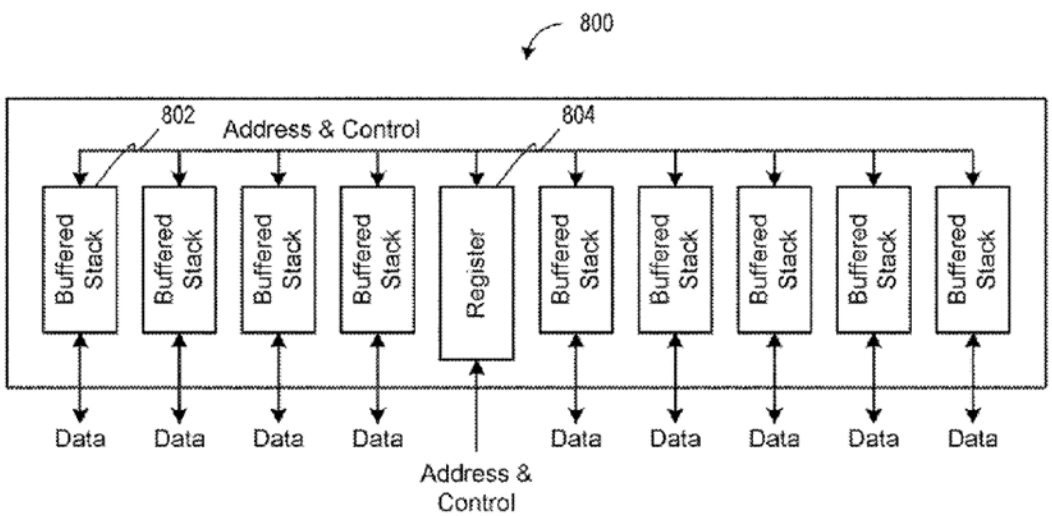


FIG. 8

e) [10.e]-[10.h.2]

The limitations [10.e]-[10.h.2] are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 1 for at least the same reasons discussed above:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[10.e]	[1.c]	¶¶380-382 (¶¶197-214)

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[10.f.1]-[10.f.2]	[1.d.1]-[1.d.2]	¶¶383-385 (¶¶215-225)
[10.g.1]	[1.e.1]	¶¶386-388 (¶¶226-234)
[10.g.2]-[10.g.3]	[1.e.2]-[1.e.3]	¶¶389-391 (¶¶235-251)
[10.h.1]-[10.h.2]	[1.e.4]-[1.e.5],[4] [10.d]	¶¶392-396 (¶¶252-266, 374-379)

9. <u>Claim 11</u>

Ground 1 teaches "*[t]he memory module of claim 10, wherein the control die receives the control signals and further includes a control circuit to control respective states of the first data conduits and the second data conduits in response to the control signals*," as discussed for claim 5 (pp.57-58). EX1003, ¶¶397-400.

10. <u>Claim 12</u>

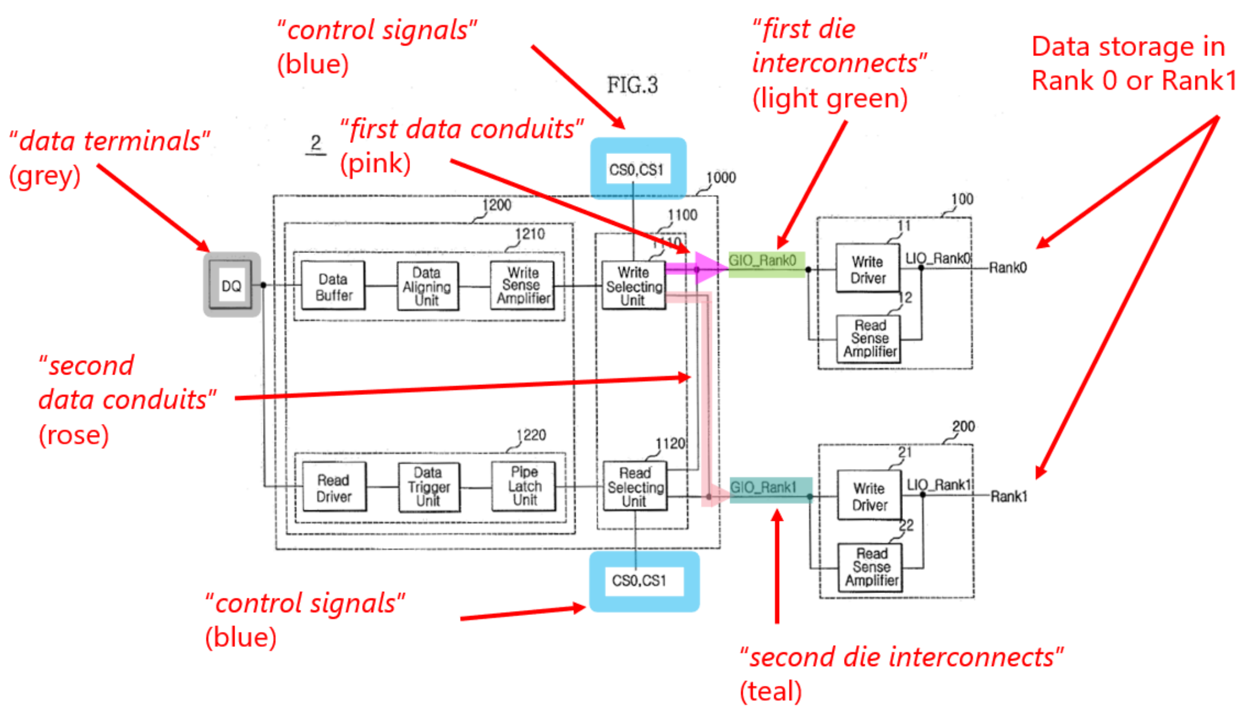
Ground 1 teaches "*[t]he memory module of claim 11, wherein the control signals* [from the "*register device*" per [10.b] (p.62)] *include data path control*

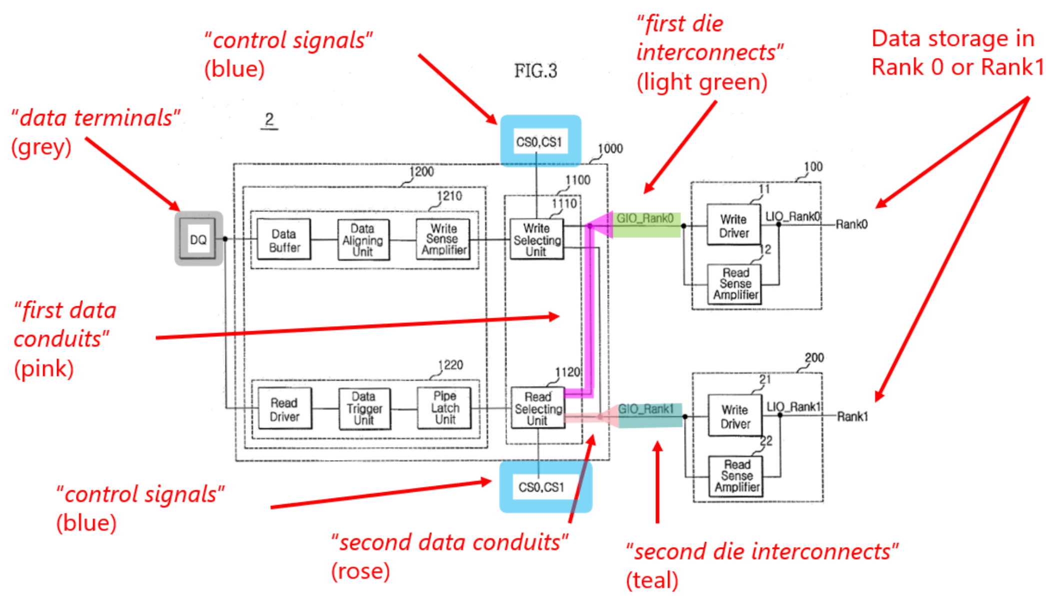
---

[4] As explained above (pp.49-53), the singular "*first data conduit*" and "*second data conduit*" in [1.e.4]-[1.e.5] lack antecedent basis, but these limitations are obvious even if interpreted as plural "*first data conduit<u>s</u>*" and plural "*second data conduit<u>s</u>*" (like in [10.h.1]-[10.h.2]) as explained above (pp.49-53). EX1003, ¶394.

signals generated by the register device [e.g., chip-select and read/write command signals pursuant to the JEDEC standard, EX1019, pp.6-14, 18, 33; EX1023, p.9, Fig.16; EX1022, pp.318-20, 332-35], *the data path control signals being used to control the respective states of the first data conduits* [(pink)] *and second data conduits* [(rose)] [including controlling the direction of the data transfer for read or write, and the selection of transferring the data through TSV1 or TSV2].”

EX1014, Fig.3 (annotated below for write (upper) and read (lower) operations); EX1003, ¶¶401-407.





A POSITA would have understood that Kim's chip selection signals and read/write command signals, received by Kim's rank selecting unit 1100 (*see* claim 5, pp.57-58), are "*data path control signals*" since they determine direction of data transfer (read or write) and select the TSVs (such as TSV1 or TSV2) through which data is transmitted from or to Rank0 or Rank1, respectively. EX1014, ¶¶[0031-38], Fig.3; EX1003, ¶404 (citing ¶¶298-306). Furthermore, Kim teaches that such "*data path control signals*" are needed to avoid collisions. EX1014, ¶[0031]; EX1003, ¶404. Moreover, in the combination of Ground 1, either the "*control circuit*" in the "*control die*" of the memory package and/or the "*register device*" (as claimed here) can implement "rank multiplication," as discussed above (pp.8-11, 30-32), thus affecting the "*data path control signals*." EX1003, ¶405.

11. Claim 13

Ground 1 teaches "*[t]he memory module of claim 11, wherein the control die* [see [1.e.1] (pp.44-45), including Kim's rank selecting unit 1100 in Figure 3, below] *is configured to generate data path control signals* [as discussed above for claim 12 (pp.65-67), including "internal write and read signals…[that are] generated," EX1014, ¶[0038]] *from at least some of the control signals* [from the "*register device*" per [10.b] (p.62), including chip selection and JEDEC-standard read/write command signals, *see* EX1014, ¶¶[0037-38]]*, the data path control signals being used to control the respective states of the first data conduits and the second data conduits* [including controlling the direction of the data transfer for read or write, and the selection of transferring the data through TSV1 or TSV2, as discussed for claim 12 (pp.65-67)]." EX1003, ¶¶401-416. As discussed above for claim 12, in the combination of Ground 1, the "*control circuit*" included in the "*control die*" in the memory package can also implement "rank multiplication," as discussed above (pp.8-11, 30-32), thus generating "*data path control signals*." EX1003, ¶414.

12. Claim 14

a) [14.a] Control Signals Include Address Signals

Ground 1 teaches "*[t]he memory module of claim 10, wherein the control signals* [from the "*register device*" per [10.b] (p.62)] *include address signals* [e.g., "Address & Control" as shown in [10.b] (p.62); *see also* EX1014, ¶[0038], which

under the JEDEC standards for read and write commands would include address signals (e.g., A0-A15) identifying where to store or retrieve the data, *see* EX1019, pp.6-13, 18, 33; EX1023, p.9, Fig.16; EX1022, pp.318-20, 332-35]." EX1003, ¶¶418-422.

b) [14.b] Control Die Provides the Address Signals

Ground 1 teaches "*the control die* [see [1.e.1] (pp.44-45), e.g., Kim's main chip C0] *provides the address signals* [from [14.a] directly above] *to the plurality of array dies* [e.g., as part of a read or write command, EX1014, ¶¶[0029-30, 32, 38], consistent with the JEDEC standards, EX1019, pp.13, 18, 33]." EX1003, ¶¶423-434. Kim teaches that main chip C0 buffers read/write commands, and corresponding address signals, and that C0 provides those buffered signals to the "*array dies*," enabling those dies to perform the corresponding read and write operations. EX1014, ¶¶[0029-30, 32, 38]; EX1003, ¶¶427-428. In addition, Rajan further makes obvious using a "*control die*" (buffer chip, green, below) to provide "*address*" and control signals (blue, below), either "altered" (e.g., by rank multiplication) or "unaltered," to the stacked "*array dies*" (yellow and orange, below). EX1015, 14:11-18, 14:55-60, Figs. 4, 18 (both below); EX1003, ¶429.

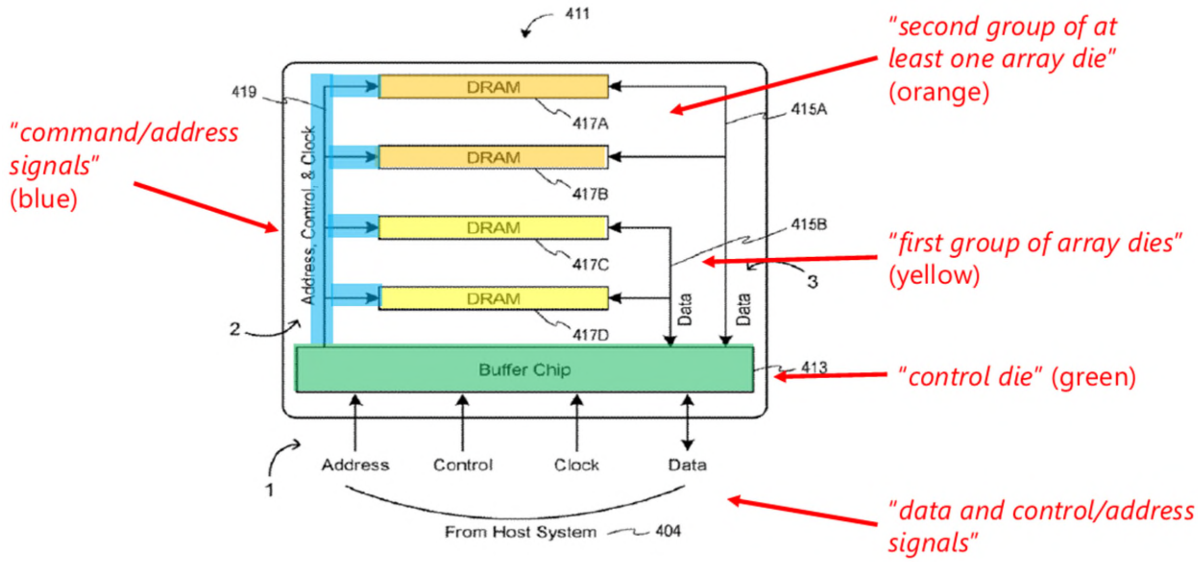


FIG. 4

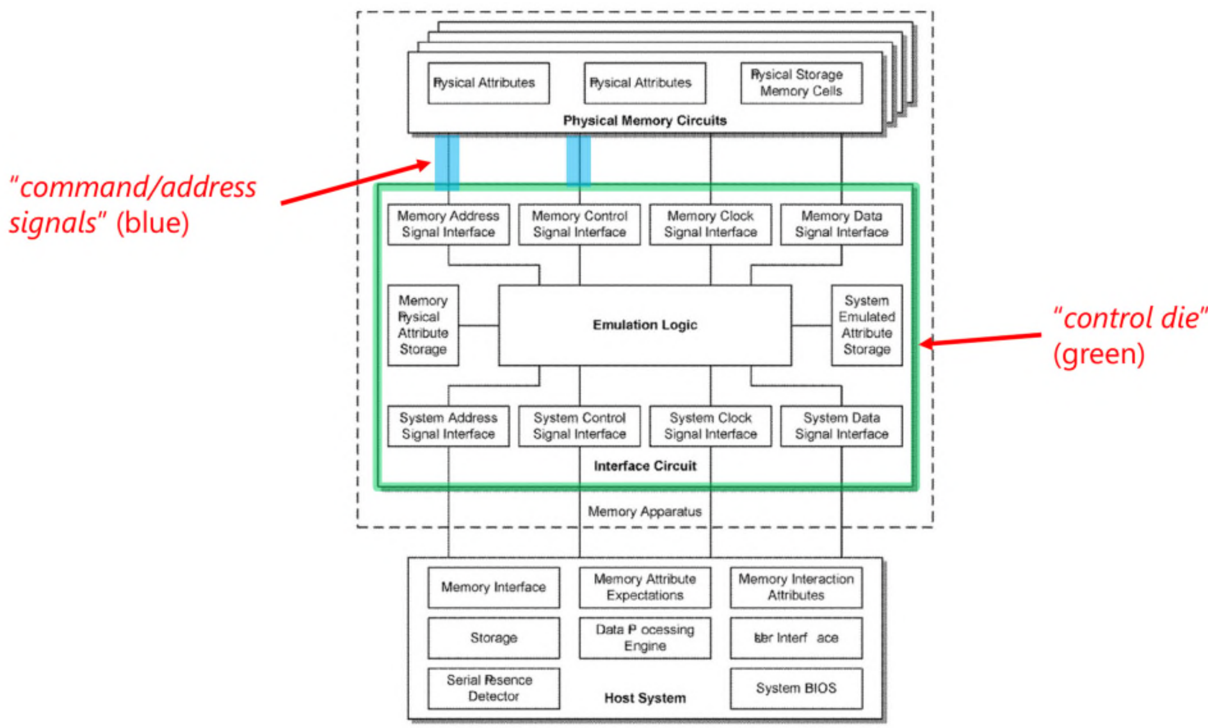
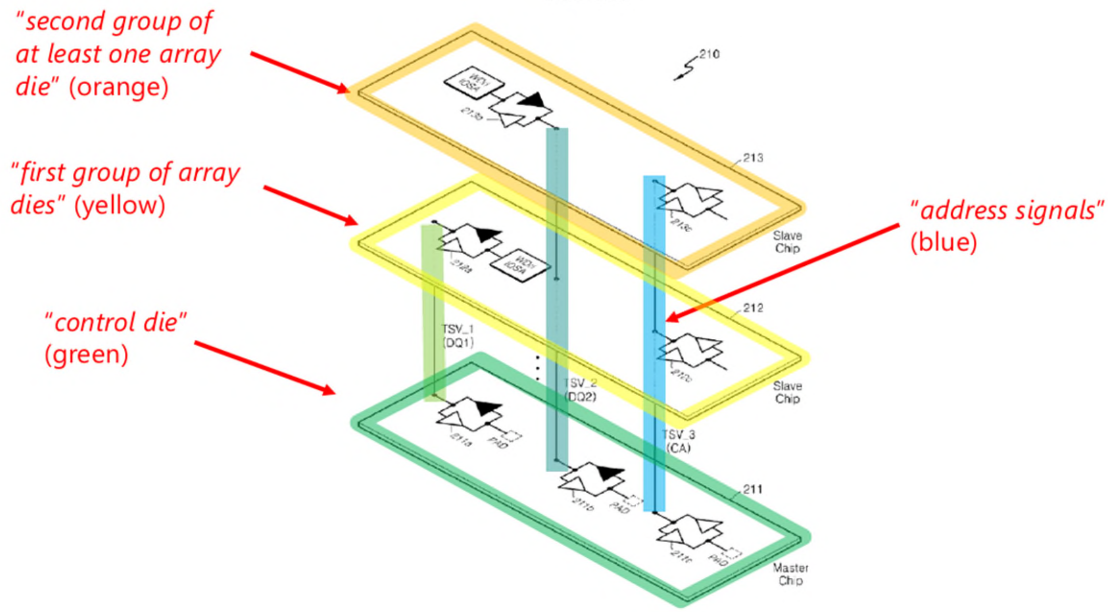


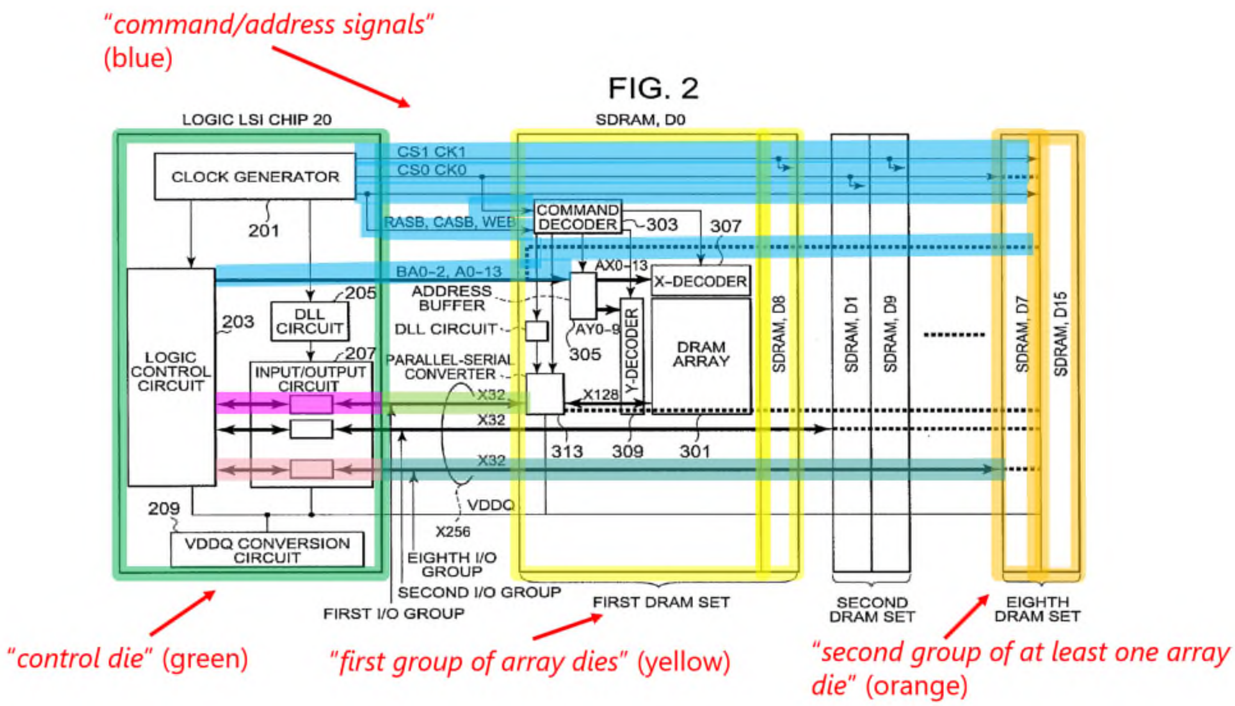
FIG. 18

Furthermore, a POSITA would have been motivated to provide command and "*address signals*" to the "*array dies*" given that it was a technique commonly used at the time, as demonstrated by the admitted prior art in the 160 Patent,

EX1001, 1:41-44, 2:7-9, Figs.1A-1B, and by other contemporaneous references such as Lee, EX1034, 21:49-52, Fig.22A (first below), and Riho, EX1016, ¶¶[0038, 0043], Fig.2 (second below), and by the JEDEC standards, EX1019, pp.13, 18, 33; EX1023, p.9, Fig.16; EX1022, pp.318-20, 332-35, resulting in nothing more than expected: having the address and command signals available at each memory chip. EX1003, ¶¶430-432.

FIG. 22A





13. <u>Claim 15</u>

a) *[15.a] Input Command/Address Signals Include First Chip Select Signals*

Ground 1 teaches "*[t]he memory module of claim 10, wherein the input command/address signals* [from [10.b] (p.62)] *include first chip select signals* [according to the JEDEC standards, EX1019, p.13 ("[Chip Select] is considered part of the command code")]." EX1003, ¶¶436-442; *see also* EX1015, 8:6-13; EX1014, ¶¶[0032, 0038].

b) *[15.b] Register Device Configured to Perform Rank Multiplication*

Ground 1 teaches "*wherein the register device* [from [10.b] (p.62)] *is configured to perform rank multiplication by generating second chip select signals* [*see* pp.8-11 (rank multiplication); EX1015, 3:27-30; 6:30-7:67, 8:56-58 ("In one

embodiment the emulation is performed at the DIMM level.")] *from at least some of the input command/address signals* [from [10.b] (p.62)], *the second chip select signals having a number of chip select signals greater than the first chip select signals* [from [15.a] directly above] *and equal to a number of array dies in the plurality of array dies* [*see* pp.8-11 (rank multiplication); EX1015, 6:34-38 (explaining that separate generated chip select signals are used for each DRAM chip in the stack)]." EX1003, ¶¶443-450. The 160 Patent also admits this was taught by the prior art. EX1001, 18:33-39, 22:19-25, Fig.7; *supra* pp.8-11.

c) [15.c] Chip Select Die Interconnects

Ground 1 teaches "*wherein the DRAM package further comprises chip select die interconnects* [e.g., between main chip C0 and slave chips C1, C2, to couple buffered chip-select signals CS0, CS1 from main chip C0 to slave chips C1 and C2, respectively, to perform read/write operations] *for conducting the second chip select signals to respective ones of the plurality of array dies*." EX1014, ¶¶[0029-30, 0049], Figs. 2, 5 (below); EX1003, ¶¶451-461.

FIG.2

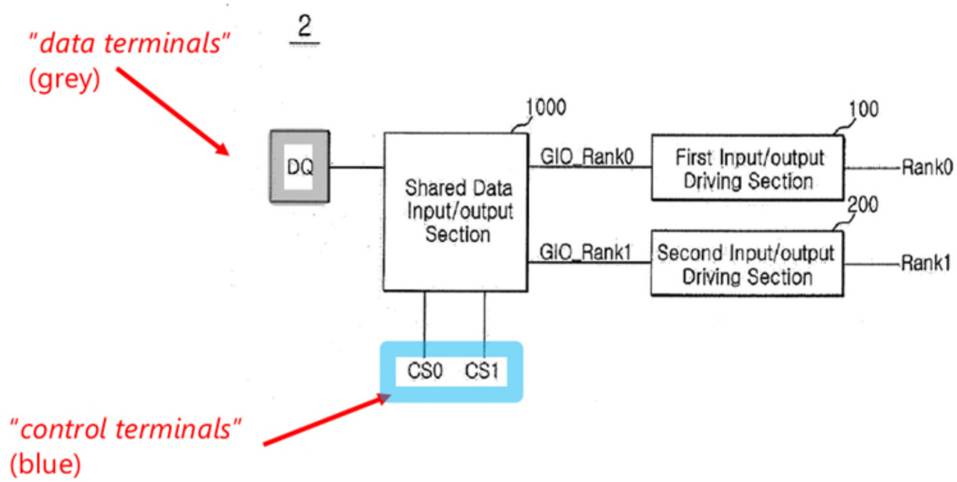
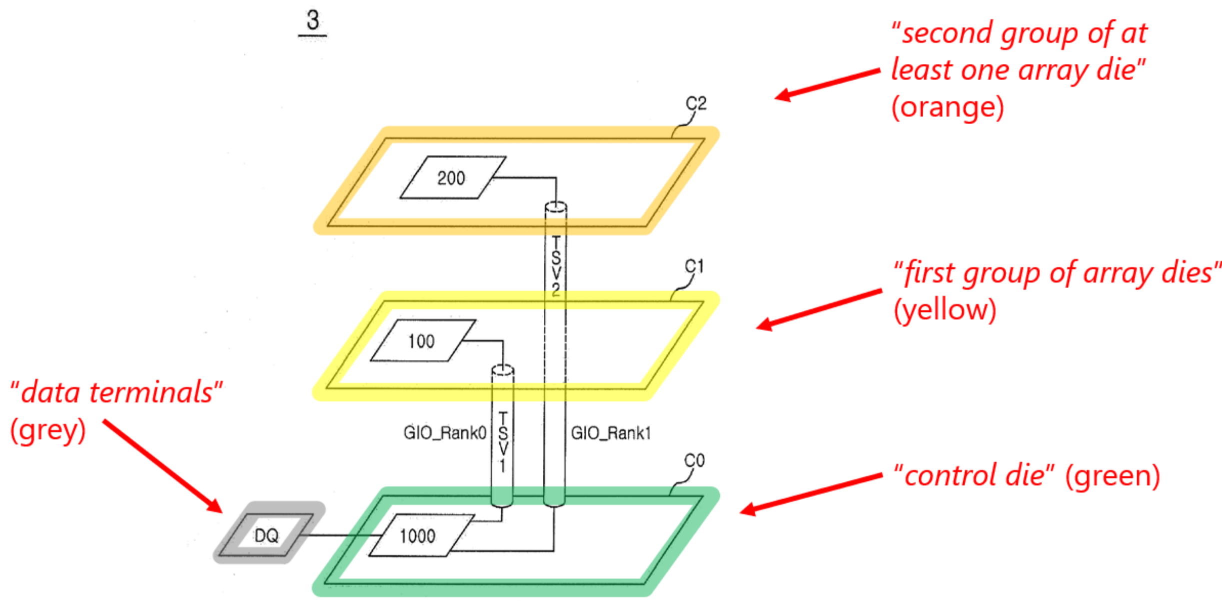


FIG.5



It would be obvious in light of <u>Kim</u>'s disclosure above to include "*chip select die interconnects*" for the chip-select signals to enable read/write operations by the "*array dies*." EX1003, ¶¶454-455. Indeed, the "chip-select bus … is essential in a JEDEC style memory system," EX1022, p.319; EX1023, pp.2-4, 9, Fig.16, and the JEDEC standard required separate chip-select signals for each

stacked memory chip (below, red), EX1019, pp.12-13, Fig.2 (below); EX1003, ¶457.

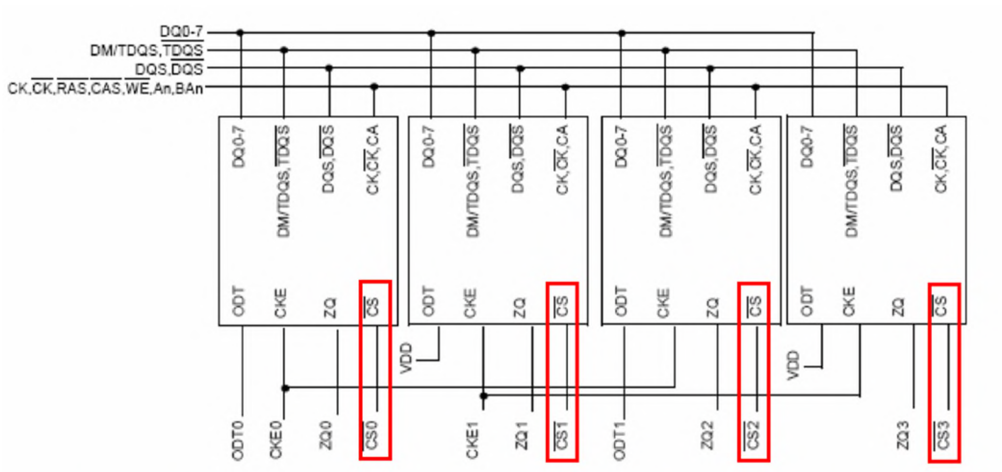


Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

Rajan further renders obvious "*chip select die interconnects*" for the chip-select signals by teaching that "extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack." EX1015, 6:34-48, Fig.4 (below); EX1003, ¶¶456-457.

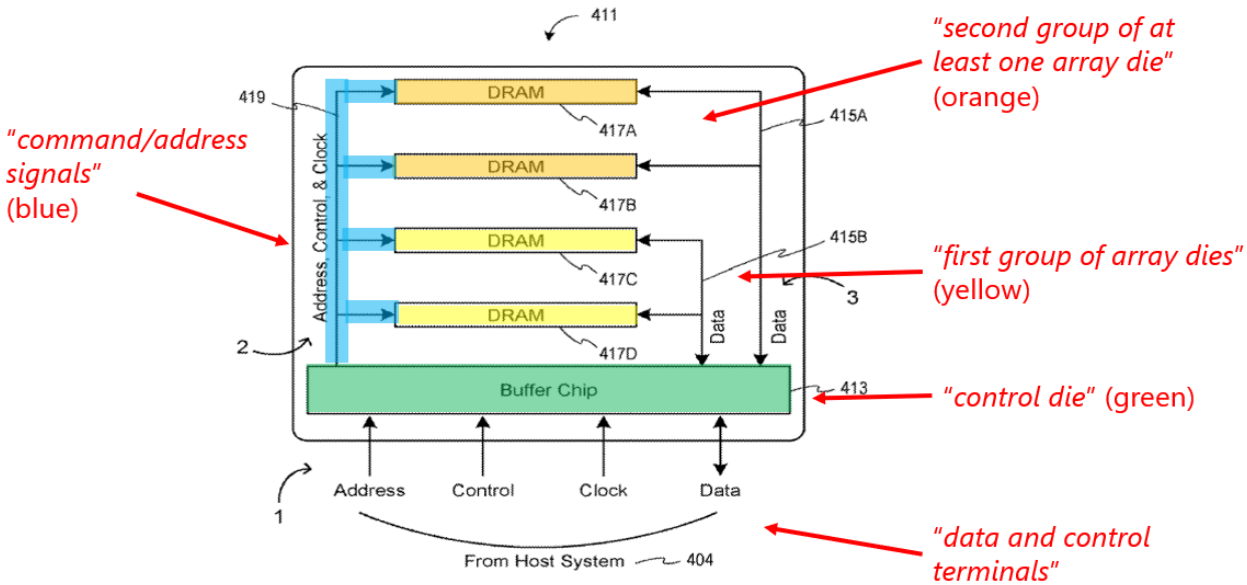


FIG. 4

Other references, including Riho and the admitted prior art in the 160 Patent, further confirm that transmitting chip-select signals through die interconnects to select a chip in the stack was well-known and within the level of skill at the time. EX1016, ¶[0038]; EX1001, 1:51-58, Figs.1A-1B; EX1003, ¶¶458-459.

14. Claim 16

a) [16.a] Control Signals Include Output Command/Address Signals Derived from the Input Command/Address Signals

Ground 1 teaches "*[t]he memory module of claim 10, wherein the control signals* [from the "*register device*" per [10.b] (p.62)] *include output command/address signals derived from the input command/address signals* [e.g., received and registered by Rajan's register 804 (below) from the *system memory controller* per [10.b] (p.62)], *the output command/address signals including first*

chip select signals [according to the JEDEC standards, EX1019, p.13 ("[Chip Select] is considered part of the command code")]." EX1015, 8:52-58, Fig. 8 (below); EX1003, ¶¶463-469; *see also* EX1022, pp.418-19 ("Registered Memory Module (RDIMM)").

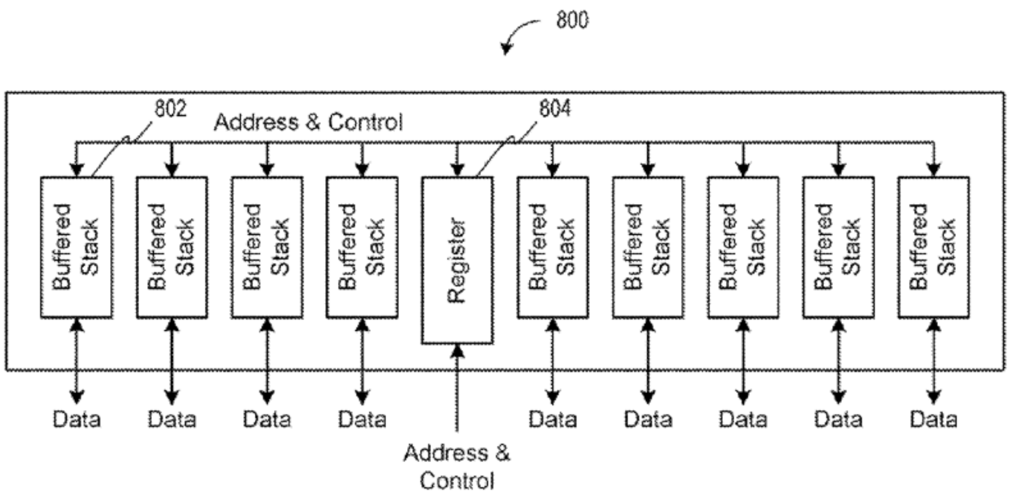


FIG. 8

b) [16.b] Control Die is Configured to Perform Rank Multiplication

Ground 1 teaches "*wherein the control die* [see [1.e.1] (pp.44-45)] *is further configured to perform rank multiplication* [see pp.8-11, 23-32] *by generating second chip select signals from at least some of the output command/address signals* [from [16.a] directly above], *the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies*," for the same reasons discussed above for [15.b] (pp.72-73), because the control circuit in the "*control*

die" of Ground 1 may also implement rank multiplication (either alternatively or in addition to the register of the module), as discussed above (pp.8-11, 30-32). EX1003, ¶¶470-473; EX1015, 6:34-38 ("In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.").

c) [16.c] Chip Select Die Interconnects

Ground 1 teaches "*wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies*," as discussed above for limitation [15.c] (pp.120-123). EX1003, ¶¶474-477.

15. <u>Claim 17</u>

Ground 1 teaches "*[t]he memory module of claim 10, wherein the first driver size and the second driver size are related to a first load on the first driver and a second load on the second driver*," as discussed above for claim 4 (p.57). EX1003, ¶¶478-482.

16. <u>Claim 18</u>

Ground 1 teaches "*[t]he memory module of claim 10, wherein the control signals include command/address signals* [see [10.b] (p.62) and [16.a] (p.76)]*, and the control die includes buffers to control the timing of the command/address signals* [e.g., <u>Rajan</u>'s buffer chip receives command/address signals for a write

command and holds those signals for "an extra two clocks of delay" to control the timing of when the stacked DRAMs receive those signals, EX1015, 9:46-10:27, Fig.11 (below)]." EX1003, ¶¶483-490. A POSITA would have been motivated by Rajan's teachings to implement this command/address signal delay in Kim's device to emulate the characteristics of JEDEC-standard memory devices, including timing. EX1015, 9:46-10:4; EX1019, pp.23-24 ("CAS latency"); EX1003, ¶488.

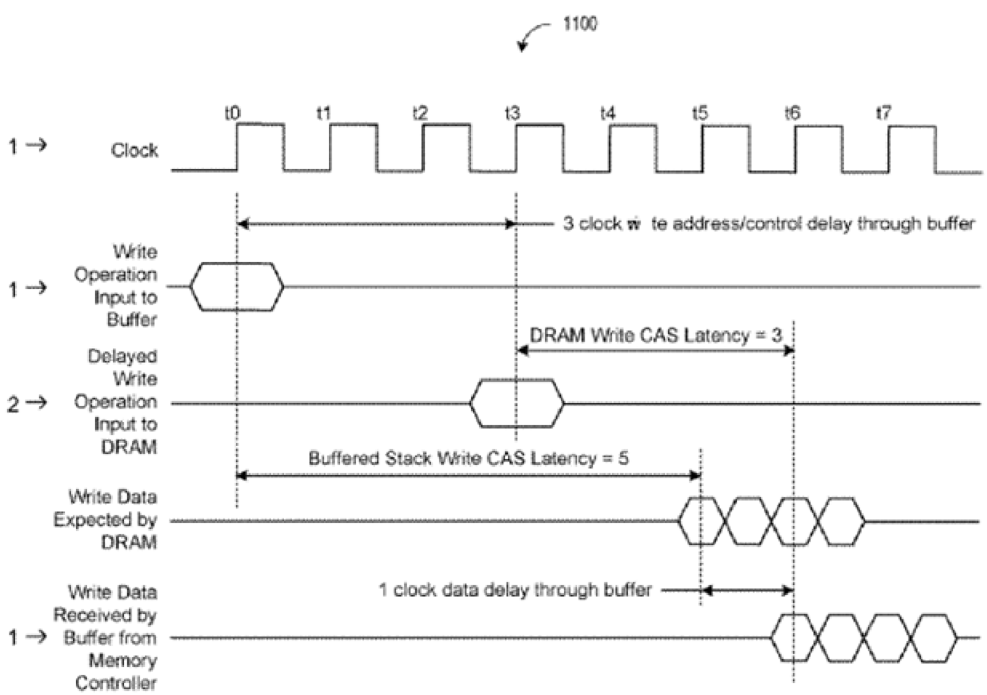


FIG. 11

17. <u>Claim 19</u>

Ground 1 teaches "*[t]he memory module of claim 10, wherein the control die includes data buffers to control the timing of the data signals* [e.g., by emulating a CAS latency to control the timing of data signals to and from the

DRAMs].” EX1015, 8:59-9:45, Fig.9[5] (below); EX1019, pp.23-24 (“CAS latency”); EX1003, ¶¶491-496; *see also* claim 18 (pp.78-79).

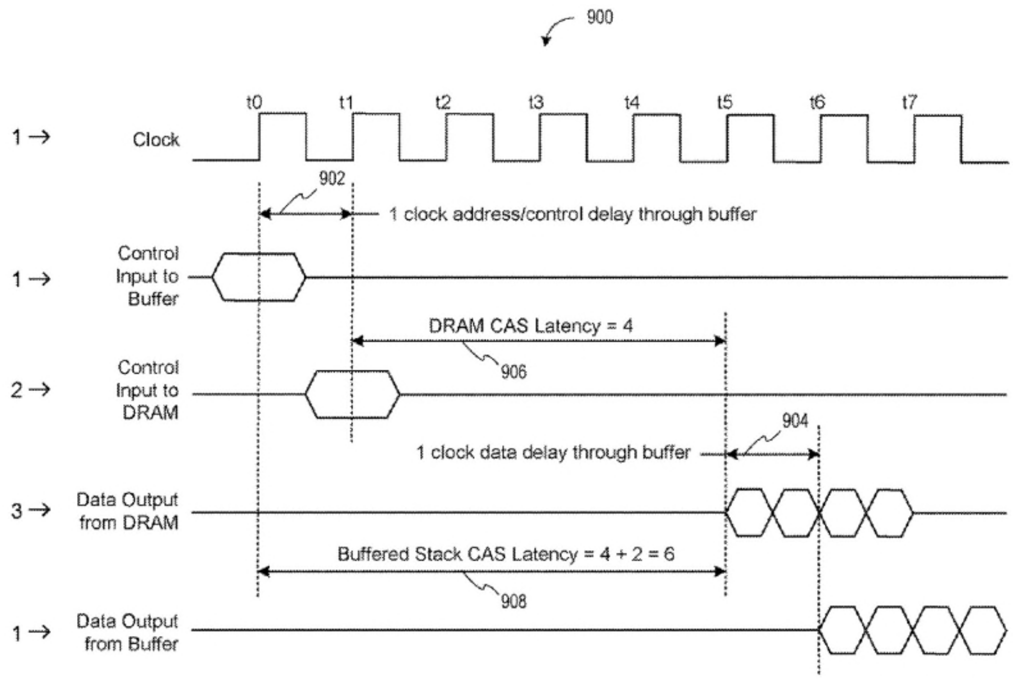


FIG. 9

18. <u>Claim 20</u>

Ground 1 teaches “*[t]he memory module of claim 10, wherein the first group of array dies include a greater number of array dies than the second group of at least one array die*,” as discussed for [3.b] (pp.55-57). EX1003, ¶¶497-501.

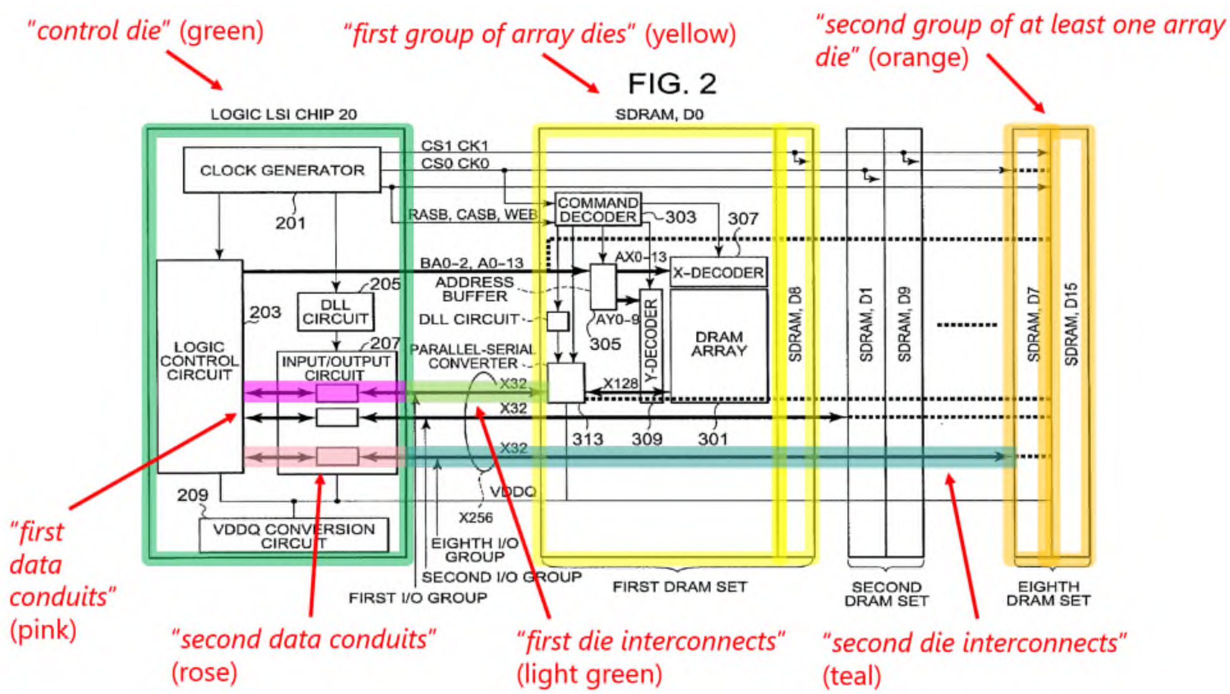
[5] Figure 9 contains a small typographical error showing CAS latency 908 ending at t5, instead of t6 as described in the specification. EX1015, 9:25-31; EX1003, ¶495.

B. Ground 2 (claims 1-20)

1. <u>Ground 2 combination: Riho (EX1016) and Rajan (1015) and Riho2 (EX1018)</u>

Ground 2 first combines <u>Riho</u> (EX1016) with <u>Rajan</u> (EX1015), both of which, like the 160 Patent, disclose the same basic memory package structure including groups of stacked memory chips (yellow, orange) and a shared interface circuit (green). EX1016, ¶¶[0002, 12], Fig.2 (first below); EX1015, 1:51-60, 2:6-7, 4:48-50, Fig.4 (second below); EX1001, 1:20-23, 5:26-29, Fig.2 (above p.14); EX1003, ¶¶503-512.

Riho:



Rajan:

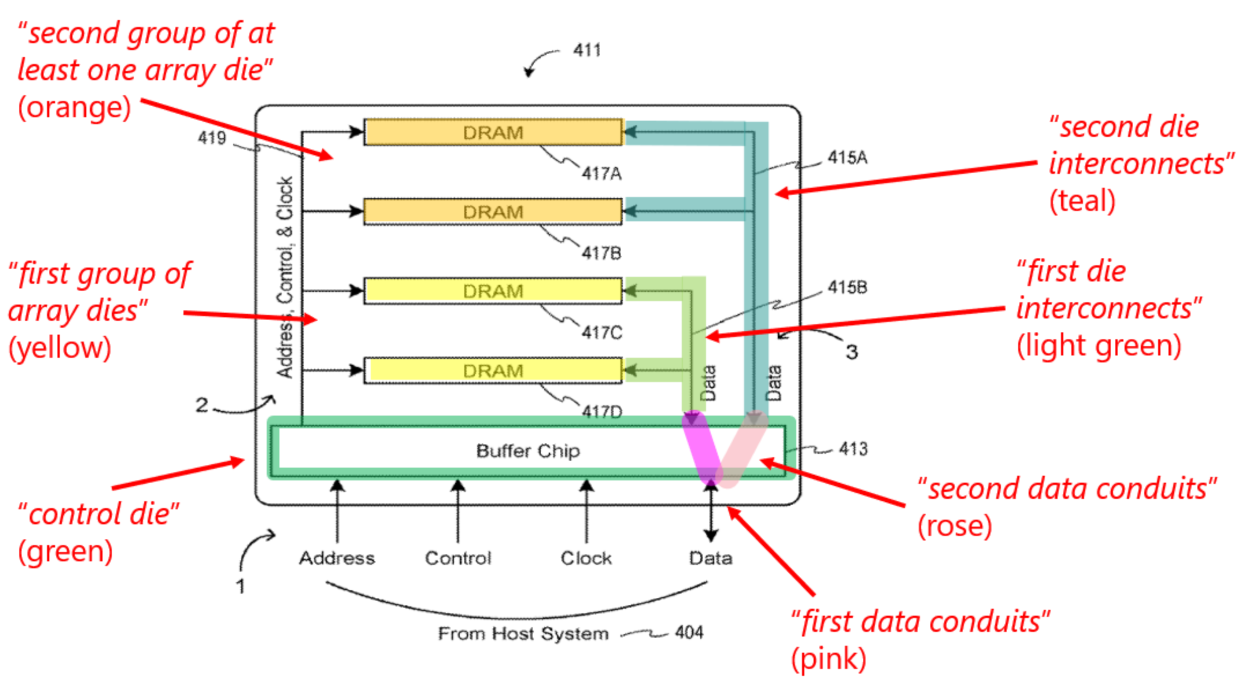


FIG. 4

A POSITA would have been motivated to combine Riho and Rajan for at least two reasons. First, as explained and shown above, they are analogous art with similar structures, so a POSITA would be motivated to look at the details taught by Rajan when implementing Riho, including details about the interface chip (green) and the external terminals to the host, which are "not illustrated" in Riho. EX1003, ¶¶505-509; EX1016, ¶¶[0026, 0030].

Second, a POSITA would be motivated to create a package with an interface that complied with the well-known JEDEC standards, as taught by Rajan. EX1003, ¶¶509-511. Specifically, a POSITA would have been motivated to look to Rajan for details about how Riho's control chip can interface with a host system — including the use of "rank multiplication" (discussed above, pp.8-11) — and to follow Rajan's suggestion to implement address, control and data terminals according to JEDEC standards (including the DDR3 standard for stacked memory devices shown below, EX1019, p.12, Fig.3, and the GDDR4 standard, EX1035, p.2). *Id.*; EX1015, 2:6-7, 3:52-54, 4:20-24, 5:36-43, 6:30-7:67, 8:8-11, Figs.4 (above), 18 (for emulation). Indeed, the JEDEC standards were influential and well-known, as discussed above (p.5).

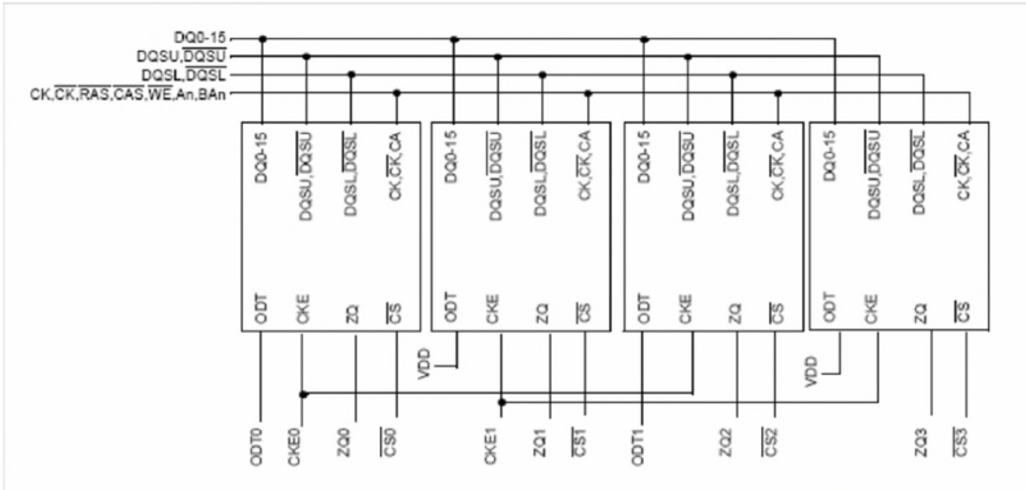
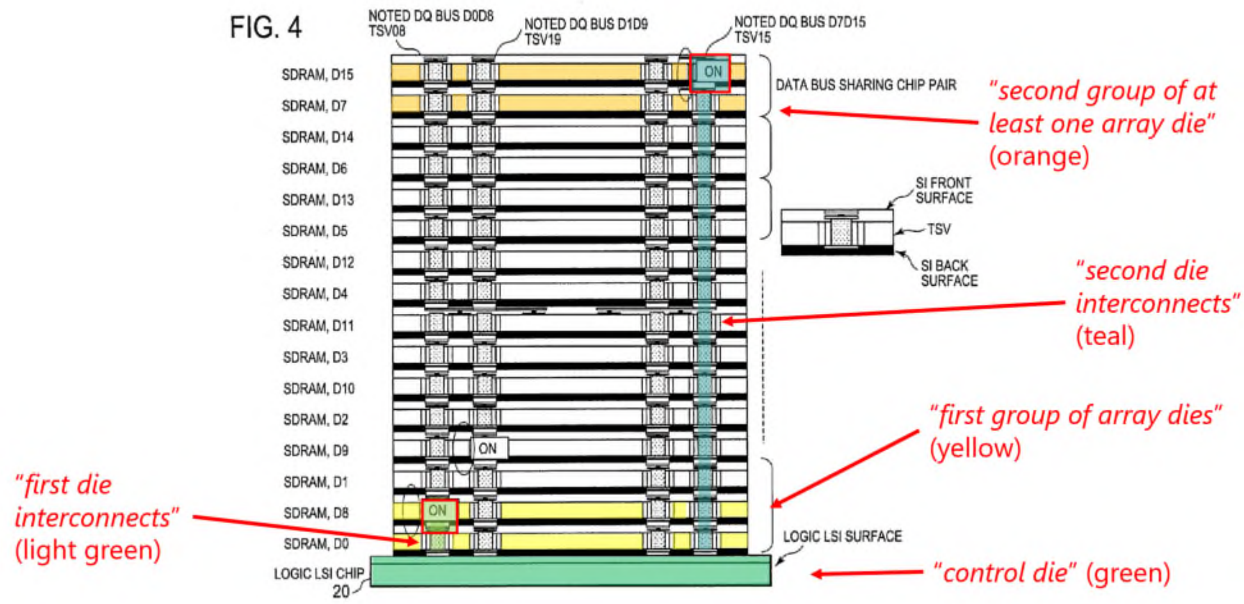


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

Such a combination would have been well within a POSITA's level of skill since emulating a standard JEDEC interface was well-known, as demonstrated by Rajan (discussed directly above) and the 160 Patent's admitted prior art (discussed above, pp.8-11). EX1003, ¶511; EX1001, 22:22-24.

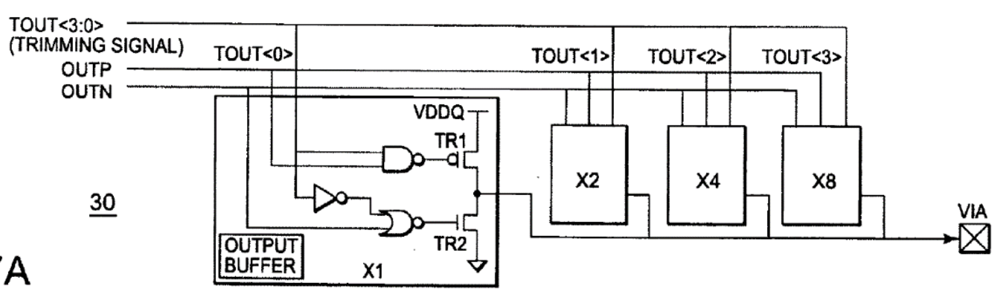
Ground 2 further combines Riho and Rajan with Riho2 (EX1018). EX1003, ¶¶503, 519-522. Riho2 is analogous art to Riho (shown below) and the 160 Patent since each is directed to improving communications between stacked chips. EX1018, ¶¶[0003, 0010], Fig.7A; EX1016, ¶¶[0002, 0012], Fig.4 (below); EX1001, 1:20-23, 5:26-29; EX1003, ¶¶514-519.

FIG. 4



Riho2 discloses a circuit (below) for optimizing output drive capacity "according to a change in the time constant caused by parasitic capacitance and parasitic resistance." EX1018, ¶¶[0003, 0010, 0097], Fig.7A (below).

FIG. 7A



A POSITA would have been motivated to combine Riho and Riho2 for at least two reasons. First, as explained above, they are closely related references with the same inventor, so a POSITA would naturally look to Riho2 for additional details about implementing Riho. EX1003, ¶¶519-520. Second, Riho discloses that impedance and resistance may vary due to variations in the TSVs and distance

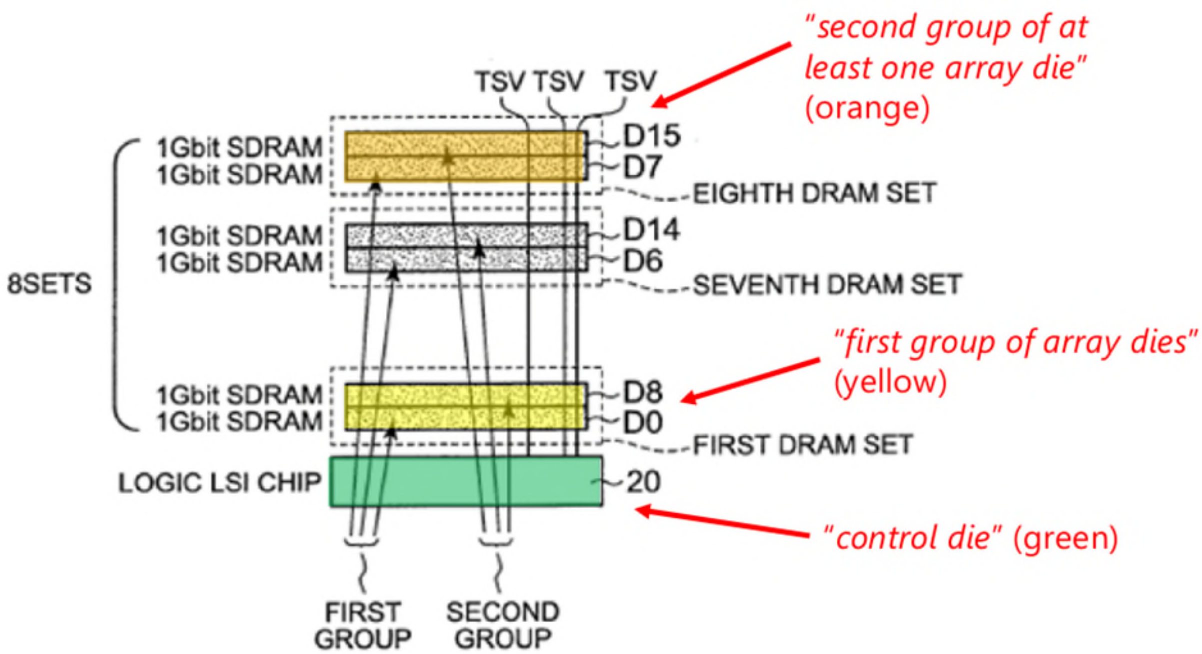
of the SDRAM chip, *see, e.g.*, EX1016, ¶¶[0055-56, 0061], and Riho2 teaches how to optimize the drive capacity of the output buffers in the control chip to account for these variations, *see, e.g.*, EX1018, ¶¶[0096-97], Fig.7A (above); EX1003, ¶¶515-518. A POSITA would be motivated to use the techniques of Riho2 to improve efficiency, and the combination would be well within the skill of a POSITA and provide the predictable result of conserving power when driving signals through Riho's TSVs. EX1003, ¶¶520-522; *see also* EX1017, 1:22-24 (utilizing the full capacity of a driver for stacked chips would be "wasteful and inefficient"), 5:11-14, Fig.5; EX1039, Abstract, 7:46-49, Fig.6.

2. Independent Claim 1

a) *[1.a] Preamble*

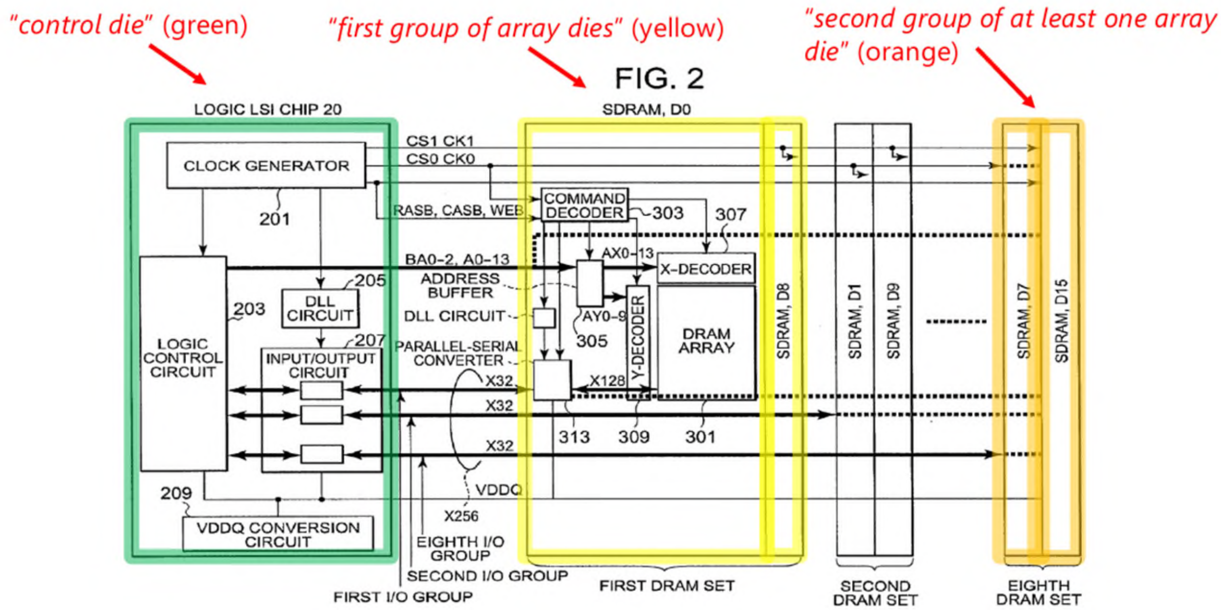
To the extent the preamble is limiting, Ground 2 teaches "*[a] memory package* [e.g., Riho's "packaged" "semiconductor device" in Figure 1 (below) including a control chip (logic LSI chip 20, green) and stacked SDRAM chips (D0-D15, yellow and orange)]*, comprising*." EX1016, ¶[0026], Fig.1 (below); EX1003, ¶¶525-529.

FIG. 1



b) [1.b] Data Terminals and Control Terminals

Ground 2 teaches "*data terminals and control terminals* [Riho's "external terminals (not illustrated)" on the "lower side" of logic LSI chip 20, green] via which the memory package communicates data [e.g., DQ signals along with related data mask, DM, and data strobe, DQS/DQSB, signals)] and control [e.g., RASB, CASB, WEB, CS0CK0, CS1CK1,…] /address [e.g., BA0-BA2 and A0-A13] signals with one or more external devices. EX1016, ¶¶[0026, 0030-31], Fig.2 (below); EX1003, ¶¶530-537; *see also* EX1019, pp.6-14, 18, 33 (JEDEC standard).



Moreover, it would have been obvious to a POSITA to implement Riho's memory package with Rajan's data and control terminals (below) to comply with the JEDEC standards, as explained above for the combination of Ground 2 (pp.81-84). EX1003, ¶¶503-512, 534-535; EX1015, Figs.4, 18 (below, illustrating a buffer chip receiving data and control/address signals from an external host system, and controlling DRAM devices in a stack).

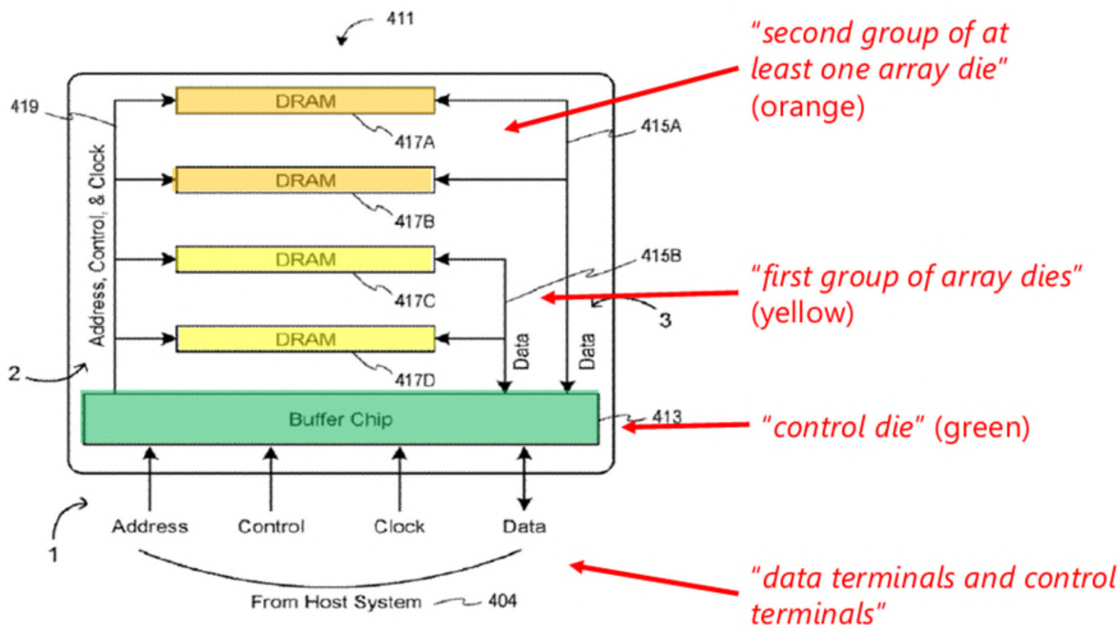

411
419
DRAM
417A
415A
DRAM
417B
DRAM
417C
415B
DRAM
417D
Address, Control, & Clock
2
Data
Data
3
Buffer Chip
413
Address
Control
Clock
Data
1
From Host System
404
"second group of at least one array die" (orange)
"first group of array dies" (yellow)
"control die" (green)
"data terminals and control terminals"

FIG. 4

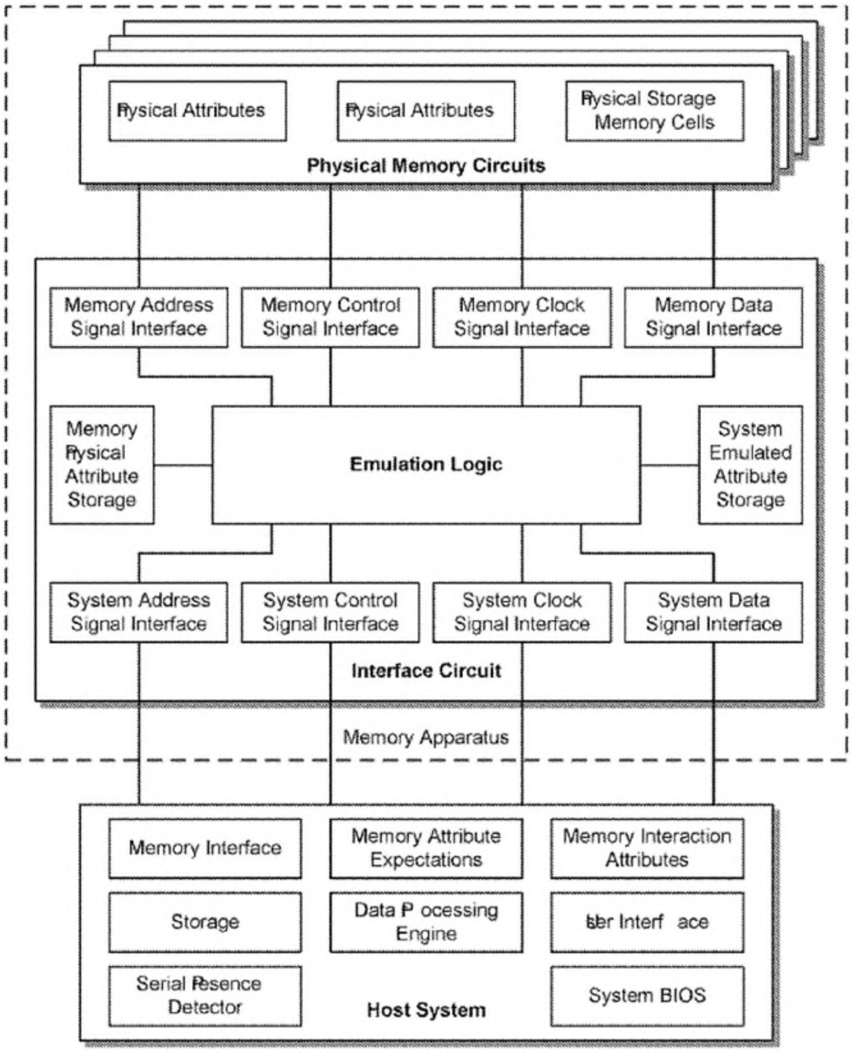


FIG. 18

c) [1.c] Stacked Array Dies

Ground 2 teaches "*stacked array dies* [e.g., SDRAM chips D0-D15, each chip including a respective DRAM array 301] *including a first group of array dies* [e.g., a first DRAM set including the pair of SDRAMs D0 and D8 sharing data signal DQ TSV08 (yellow)] *and a second group of at least one array die* [e.g., an eighth DRAM set including the pair of SDRAMs D7 and D15 sharing data signal DQ TSV715 (orange)]." EX1016, ¶¶[0027, 0029, 0045-47, 0049, 0062], Figs.1-2

(below); EX1003, ¶¶538-545. A POSITA would understand that Riho's SDRAM chip includes a "die." EX1018, Abstract, Fig.1 ("stacked" "chip die[s]"); EX1003, ¶542.

FIG. 1

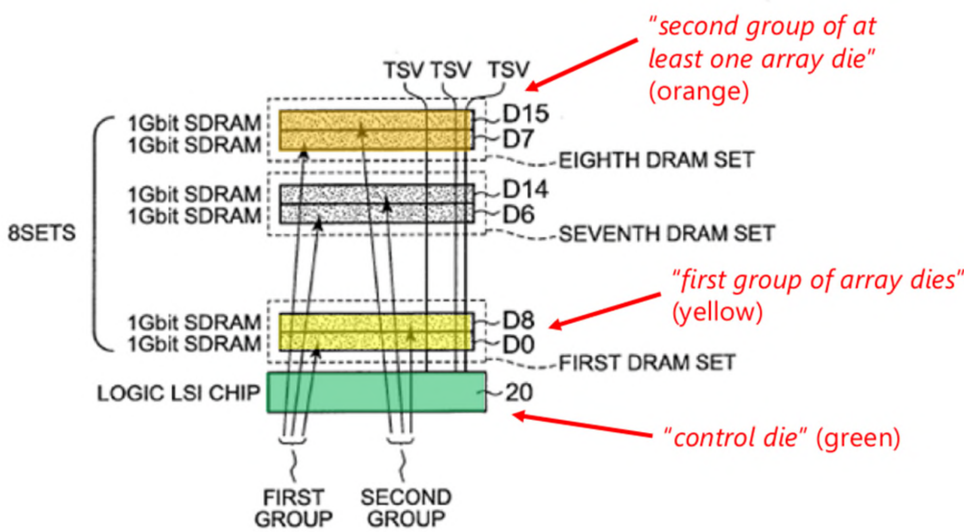
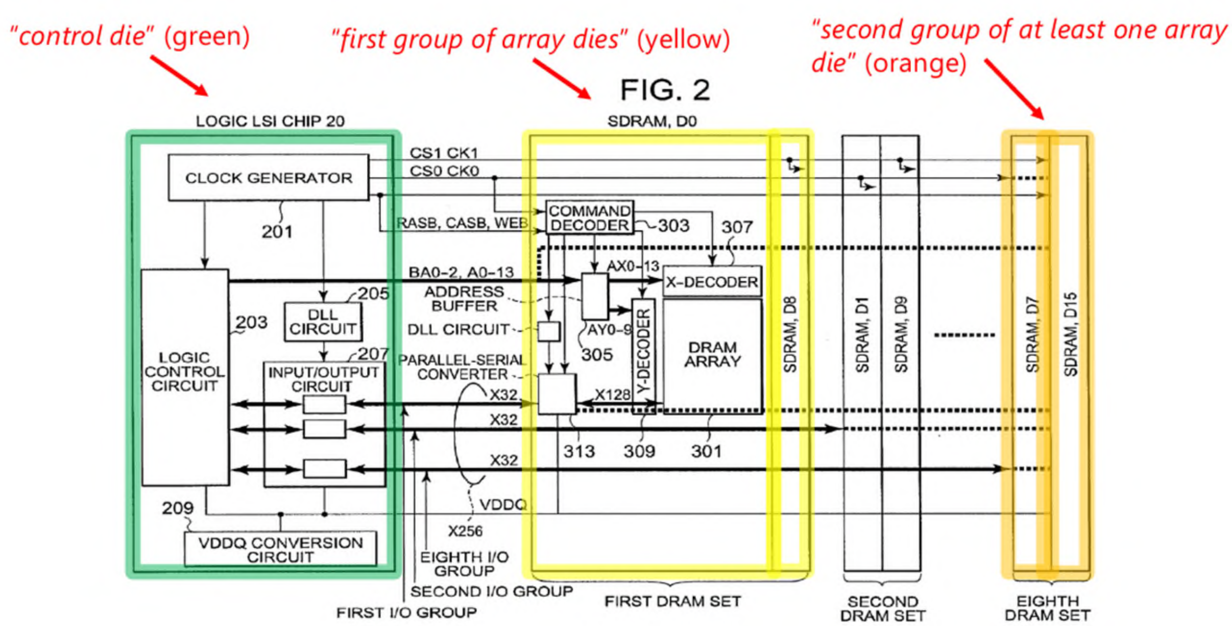


FIG. 2



d) [1.d.1]-[1.d.2] Die Interconnects in Electrical Communication with Array Dies

Ground 2 teaches "*first die interconnects* [e.g., data signal DQ TSV08 (light green)] *and second die interconnects* [e.g., data signal DQ TSV715 (teal)], *the first die interconnects* [TSV08] *in electrical communication with the first group of array dies* [e.g., the first DRAM set including SDRAMs D0 and D8 (yellow) are in a "conductive" (i.e., "on") state] *and not in electrical communication with the second group of at least one array die* [e.g., all other SDRAMs, including the eighth DRAM set of SDRAMs D7 and D15 (orange), are in a "non-conductive" (i.e., "off") state]," and "*the second die interconnects* [TSV715] *in electrical communication with the second group of at least one array die* [including SDRAMs D7 and D15] *and not in electrical communication with the first group of array dies* [including SDRAMs D0 and D8]." EX1016, ¶¶[0045-46, 0064-65], Figs.2, 4 (both below); EX1003, ¶¶546-563. Rajan also teaches this arrangement to reduce load (third below), further rendering obvious [1.d.1]-[1.d.2]. EX1015, 5:36-43, 5:63-6:2, Fig.4 (third below); EX1003, ¶¶558-562.

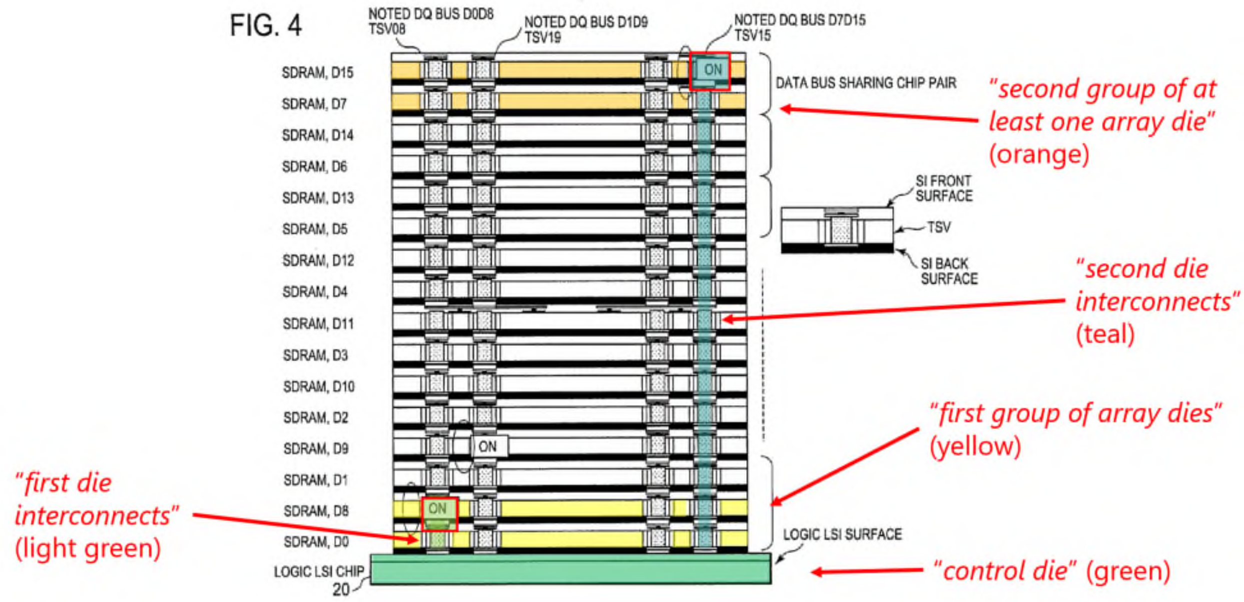
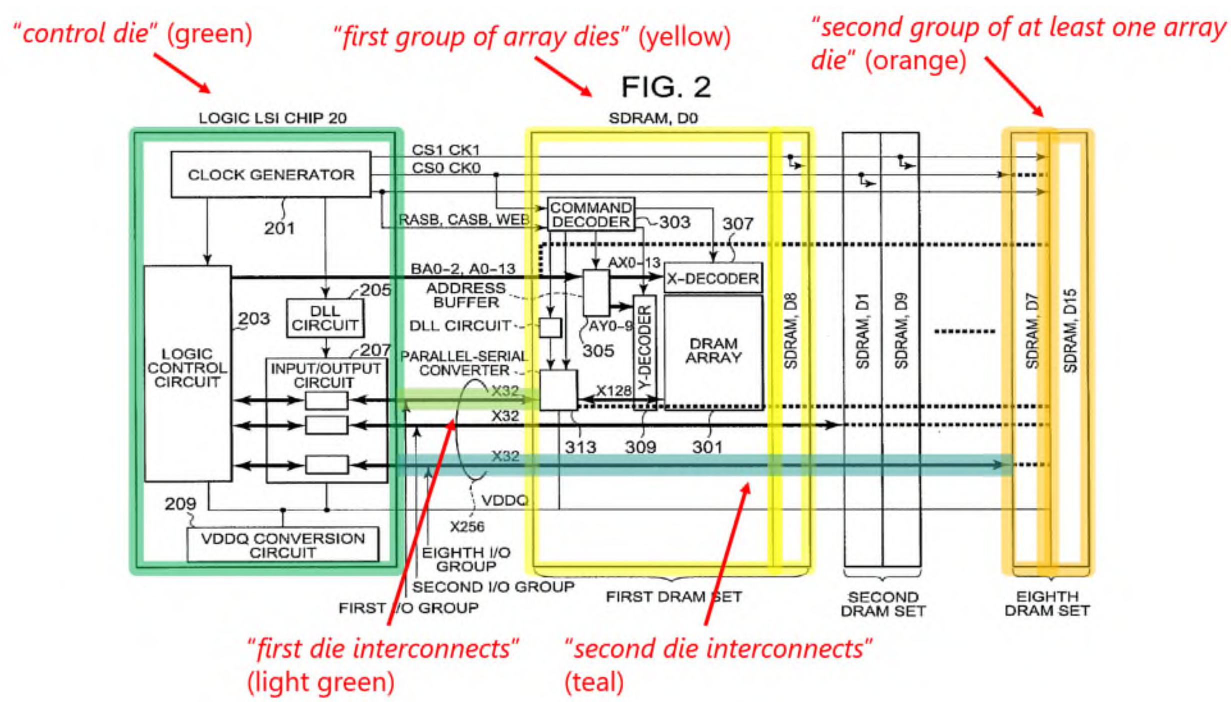


FIG. 4
NOTED DQ BUS D0D8 TSV08
NOTED DQ BUS D1D9 TSV19
NOTED DQ BUS D7D15 TSV15
SDRAM, D15
SDRAM, D7
SDRAM, D14
SDRAM, D6
SDRAM, D13
SDRAM, D5
SDRAM, D12
SDRAM, D4
SDRAM, D11
SDRAM, D3
SDRAM, D10
SDRAM, D2
SDRAM, D9
SDRAM, D1
SDRAM, D8
SDRAM, D0
LOGIC LSI CHIP 20
ON
ON
ON
DATA BUS SHARING CHIP PAIR
SI FRONT SURFACE
TSV
SI BACK SURFACE
LOGIC LSI SURFACE
"second group of at least one array die" (orange)
"second die interconnects" (teal)
"first group of array dies" (yellow)
"first die interconnects" (light green)
"control die" (green)


"control die" (green)
"first group of array dies" (yellow)
"second group of at least one array die" (orange)
FIG. 2
LOGIC LSI CHIP 20
SDRAM, D0
CLOCK GENERATOR
201
CS1 CK1
CS0 CK0
RASB, CASB, WEB
COMMAND DECODER
303
307
BA0–2, A0–13
AX0–13
X-DECODER
ADDRESS BUFFER
205
DLL CIRCUIT
203
DLL CIRCUIT
AY0–9
305
Y-DECODER
DRAM ARRAY
207
LOGIC CONTROL CIRCUIT
INPUT/OUTPUT CIRCUIT
PARALLEL-SERIAL CONVERTER
X32
X32
X32
X128
313
309
301
209
VDDQ
X256
VDDQ CONVERSION CIRCUIT
EIGHTH I/O GROUP
SECOND I/O GROUP
FIRST I/O GROUP
FIRST DRAM SET
SECOND DRAM SET
EIGHTH DRAM SET
SDRAM, D8
SDRAM, D1
SDRAM, D9
SDRAM, D7
SDRAM, D15
"first die interconnects" (light green)
"second die interconnects" (teal)

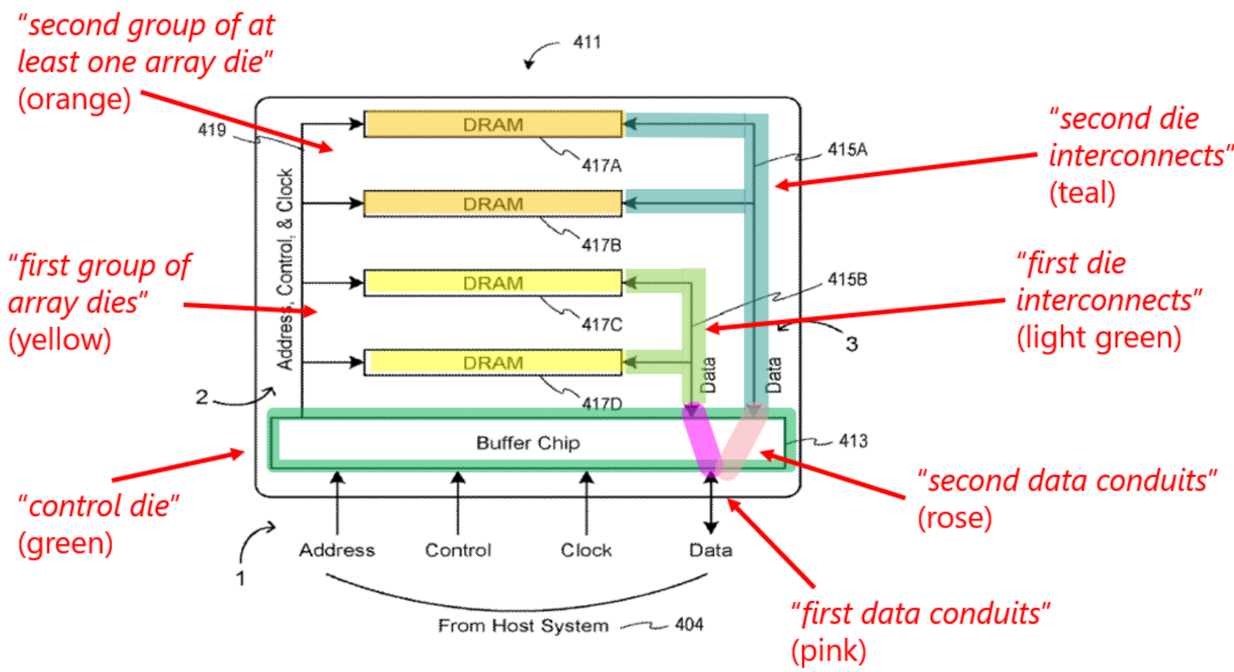
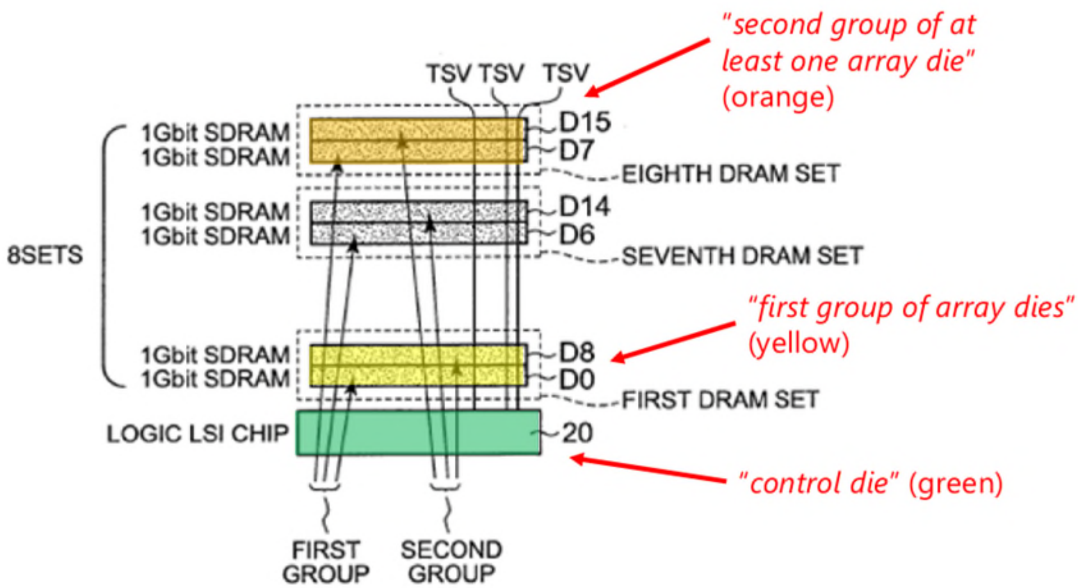


FIG. 4

e) [1.e.1] Control Die

Ground 2 teaches "*a control die* [e.g., Riho's Logic LSI chip 20 (green), described as "a control chip"] *comprising*." EX1016, ¶[0026], Fig.1 (below); EX1003, ¶¶564-571. As discussed above (pp.81-84), the "*control die*" in the combination of Ground 2 may emulate one or more characteristics, such as the number of ranks (e.g., for "rank multiplication"), that are different from the characteristics of the physical memory devices. EX1003, ¶569.

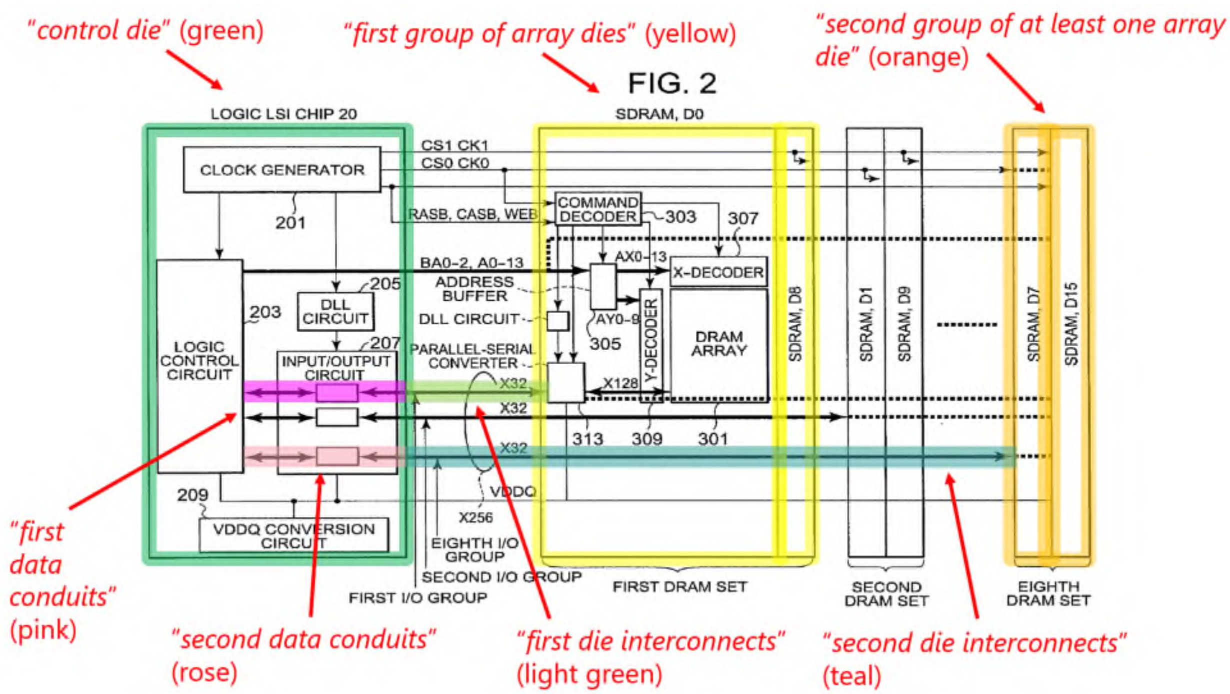
FIG. 1



f) *[1.e.2]-[1.e.3] First and Second Data Conduits*

Ground 2 teaches "*first data conduits* [(pink)] *between the first die interconnects* [DQ TSV08 (light green)] *and the data terminals* [from [1.b] (pp.87-90)], *and second data conduits* [(rose)] *between the second die interconnects* [DQ TSV715 (teal)] *and the data terminals*." EX1016, Fig.2 (annotated below); EX1003, ¶¶572-588. In particular, Riho discloses "external terminals (not illustrated)" and that "logic circuit 203 provided in the logic LSI chip 20…sends and receives data signals DQ between itself and the input/output circuit 207," and refers to those data signals as an "I/O group," indicating that control chip 20 (green, below) has external input/output "*data terminals*" for communicating data

signals via "*data conduits*" (pink, rose, below) to the array dies. EX1016, ¶¶[0026, 0039-40, 0045-46], Fig.2 (below); EX1003, ¶¶575-581.



Furthermore, as explained above (pp.81-84), a POSITA would have been motivated to look to Rajan for details about how Riho's control chip can interface with a host system pursuant to the JEDEC standards, and Rajan discloses external terminals for data signals (below) that comply with the JEDEC standards. EX1015, 2:6-7, 3:52-54, 4:20-24, 5:36-43, 8:8-11, Figs.4, 18 (below); EX1019, p.12; EX1035, p.2; EX1003, ¶¶582-585. Rajan also teaches that the "*first*" (pink) and "*second*" (rose) "*data conduits*" would be coupled to the "*data terminals*" at the bottom of the buffer chip ("*control die*"), as shown below. *Id.*; EX1003, ¶¶582, 585-586; *see also* pp.8-11, 31-32.

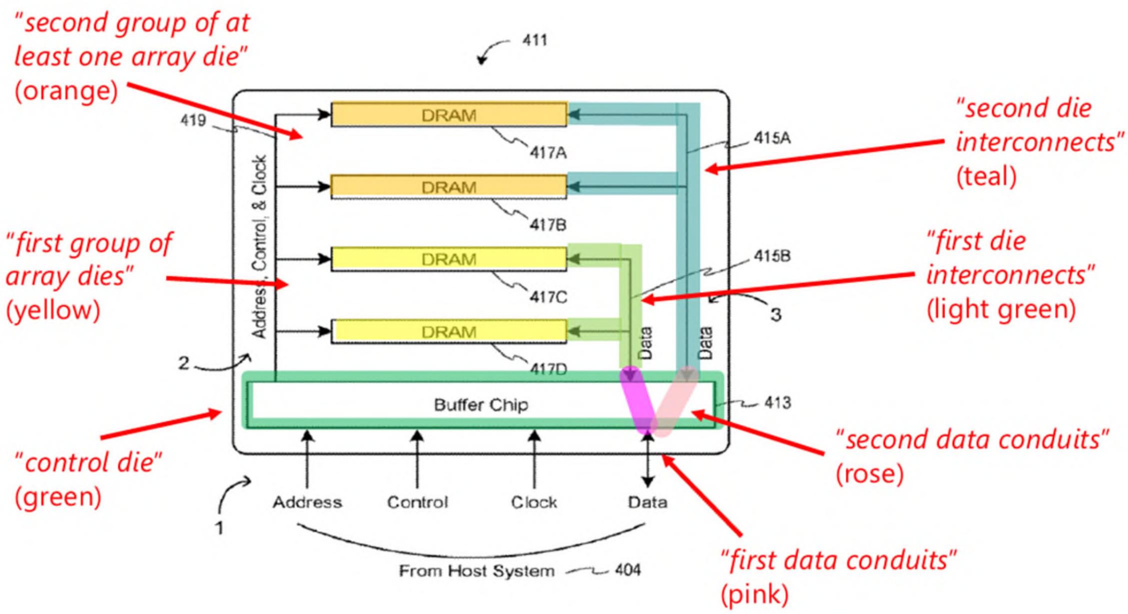

"second group of at least one array die" (orange)
411
419
DRAM
417A
DRAM
417B
DRAM
417C
DRAM
417D
415A
"second die interconnects" (teal)
"first group of array dies" (yellow)
Address, Control, & Clock
415B
3
"first die interconnects" (light green)
Data
Data
2
Buffer Chip
413
"second data conduits" (rose)
"control die" (green)
Address
Control
Clock
Data
1
From Host System
404
"first data conduits" (pink)

FIG. 4

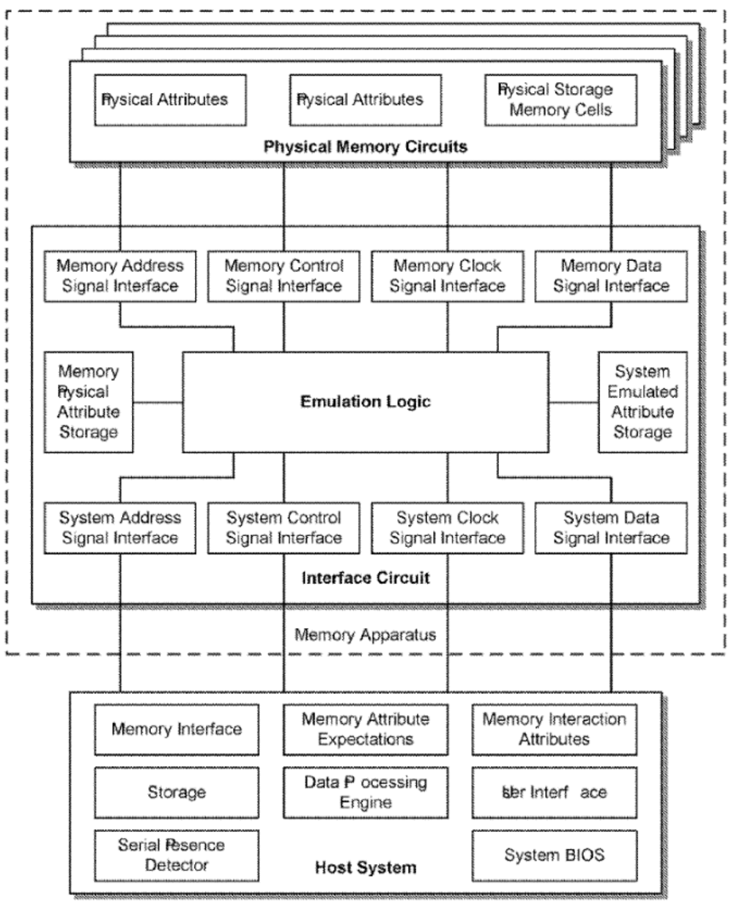
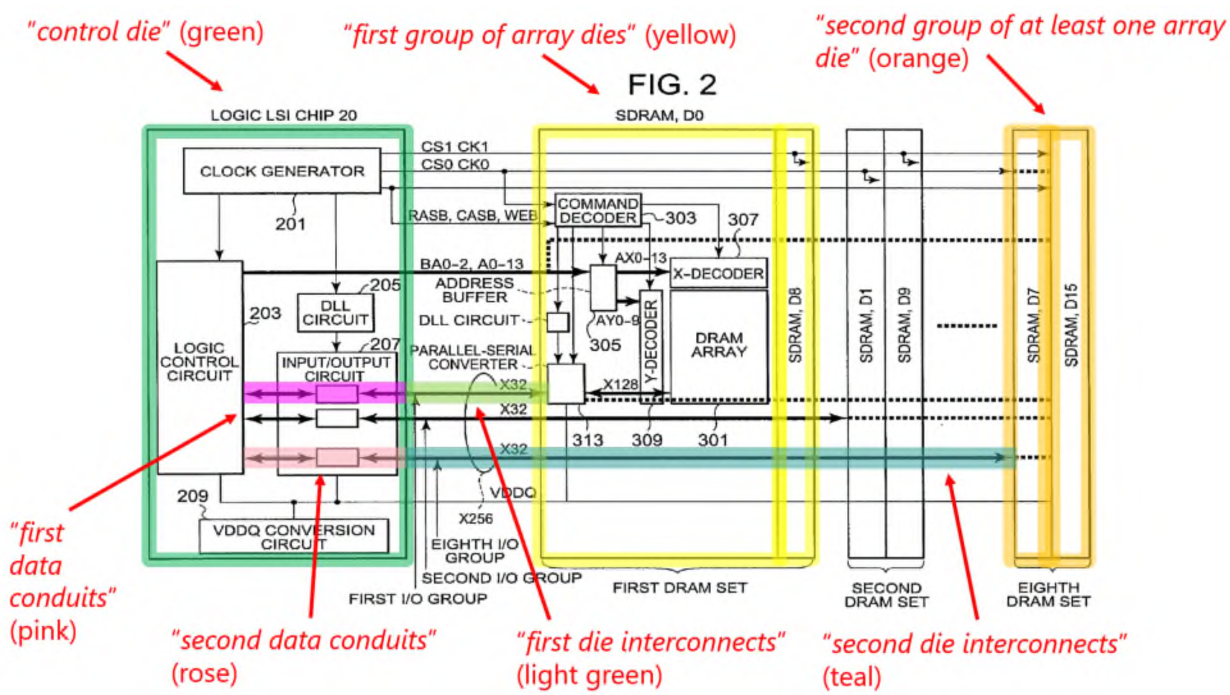

Physical Attributes
Physical Attributes
Physical Storage Memory Cells
Physical Memory Circuits
Memory Address Signal Interface
Memory Control Signal Interface
Memory Clock Signal Interface
Memory Data Signal Interface
Memory Physical Attribute Storage
Emulation Logic
System Emulated Attribute Storage
System Address Signal Interface
System Control Signal Interface
System Clock Signal Interface
System Data Signal Interface
Interface Circuit
Memory Apparatus
Memory Interface
Memory Attribute Expectations
Memory Interaction Attributes
Storage
Data Processing Engine
User Interface
Serial Presence Detector
Host System
System BIOS

FIG. 18

g) [1.e.4]-[1.e.5] First and Second Drivers

Ground 2 teaches "*the first data conduit* [(pink)] *including first drivers* [in input/output circuit 207, as explained further in the next paragraph] *each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies* [including SDRAM chips D0 and D8]," and "*the second data conduit* [(rose)] *including second drivers* [in input/output circuit 207, as explained further in the next paragraph] *each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die* [including SDRAM chips 7 and 15]*, the second driver size being different from the first driver size* [as explained further below]." EX1003, ¶¶589-606. The claim limitations "*the first data conduit*" and "*the second data conduit*" lack proper antecedent basis given that [1.e.2]-[1.e.3] recite "*first data conduit**s***" and "*second data conduit**s***." EX1003, ¶590. Nevertheless, it would be obvious in light of Ground 2 that each "*data conduit*" could include one or more "*drivers*," as explained further below, thus rendering the claimed "*data conduit[s]*" obvious either way despite the lack of proper antecedent basis. *Id.*

FIG. 2



With respect to the "*data conduit[s]*" including "*drivers*": Drivers were well-known (pp.6-8), and it would be obvious to a POSITA from Riho's disclosure that "[e]ach input/output circuit 207 sends and receives 32-bit width data signals DQ between itself and the SDRAMs D0 to D15 …. [using] interface circuits such as buffers" to use "*driver[s]*" in the "*data conduit[s]*" to produce enough current to transmit the data signals from one chip ("*control die*") to another chip ("*array die*"). EX1016, ¶¶[0040, 0045-46]; EX1030, pp.135-36 ("buffers are…used when high current flow is needed to drive external devices"); EX1038, p.68 ("tri-state drivers" are "commonly used"); EX1003, ¶¶591-597.

With respect to the driver sizes "*being different*": Riho teaches that manufacturing variations in the TSVs, including impedances, and different

positions of SDRAM chips in the stack, should be accounted for when designing Riho's stacked structure, *see* EX1016, ¶¶[0055-56, 0061], and a POSITA would have been motivated by Riho2 to account for these variations by selectively activating one or more drivers (below) to achieve the optimal driving strength for each "*data conduit*," thus saving power, *see* EX1018, ¶¶[0096-97], Fig.7A (below); *see also* EX1017, 1:22-24, 5:11-14, Fig.5. EX1003, ¶¶598-603.

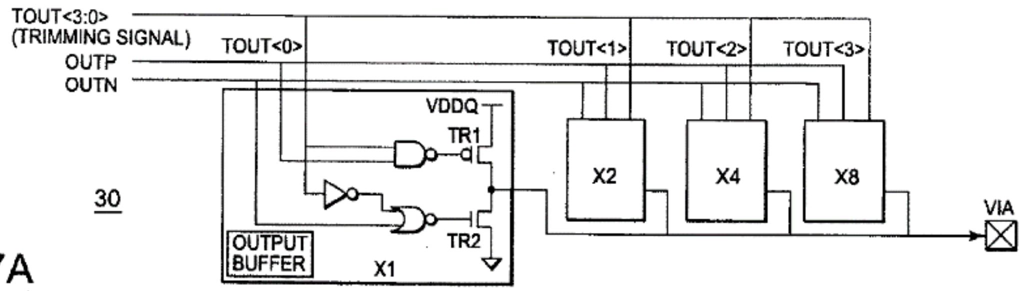


FIG. 7A

Other contemporaneous references confirm that adjusting the driver strength to account for the position of a die in stack was well known at the time. EX1039, Abstract, 7:46-49 (describing a compensation circuit "compensate[ing] for both termination impedance and drive strength variations resulting from differences in die location"); Fig.6 (below). EX1003, ¶604.

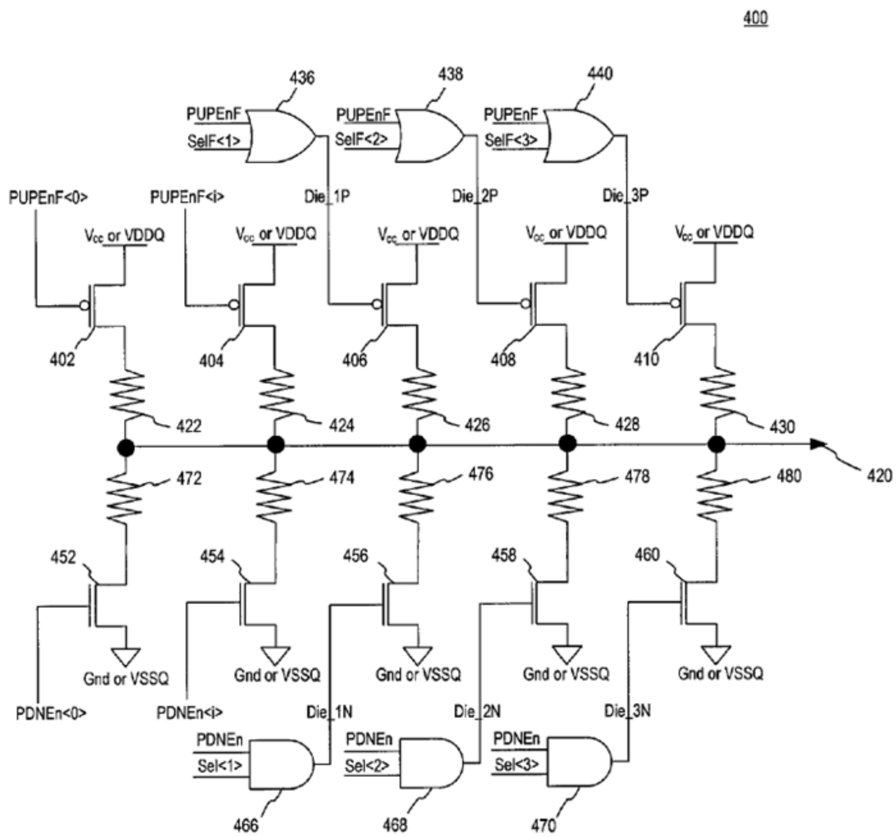
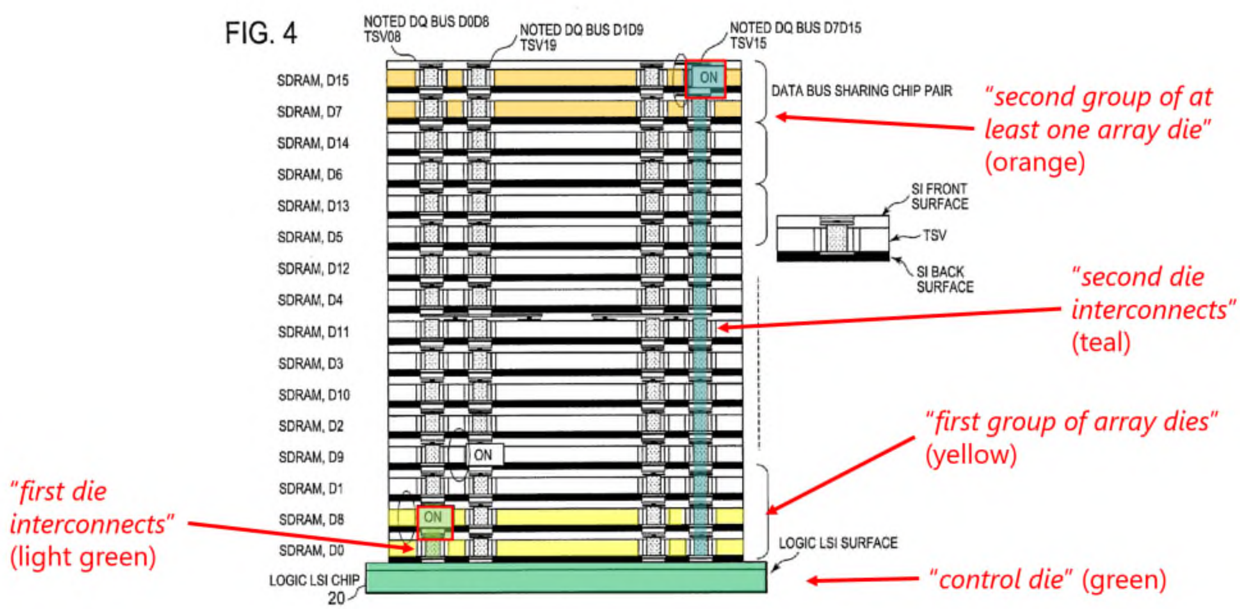


Figure 6

3. Claim 2

Ground 2 teaches "*[t]he memory package of claim 1, wherein the second die interconnects* [e.g., TSV715 (teal below)] *are longer than the first die interconnects* [TSV08 (light green below)] [since SDRAM chips D7/D15 coupled to TSV715 are farther away from control chip 20 than SDRAM chips D0/D8 coupled to TSV08, *see* EX1016, Fig.4 (first below)] *and wherein the second driver size is larger than the first driver size* [because SDRAM chips D7/D15 are farther away, resulting in greater "penetrating through resistance" according to Riho,

EX1016, ¶[0061], and thus requiring a larger driver size, as taught by Riho2, EX1018, ¶[0097], Fig.7A; EX1039, 8:21-48; EX1017, 6:15-30].” EX1003, ¶¶607-616; *see also supra* pp.98-101. Rajan also teaches that the “*second die interconnects*” are longer than the “*first die interconnects*,” as shown below, EX1015, Fig.4 (second below), and a POSITA would have been motivated to implement that arrangement to reduce the load of the “*first die interconnects*,” EX1017, 1:22-24, thus further rendering obvious claim 2. EX1003, ¶¶612-613.



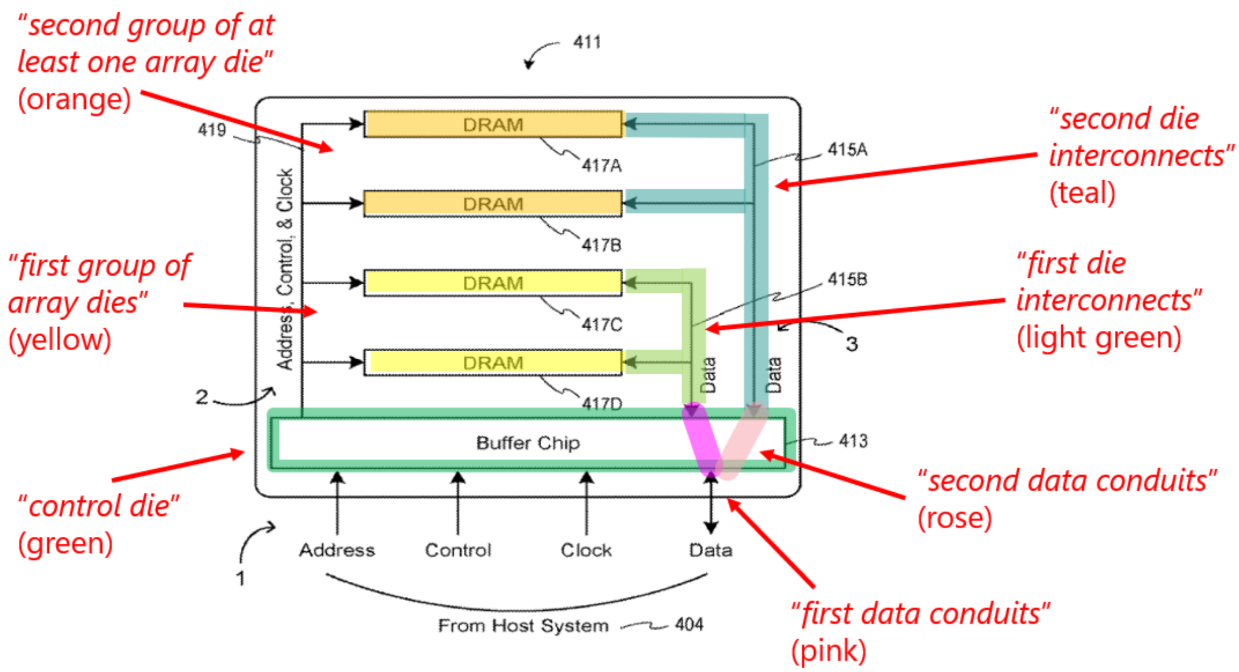


FIG. 4

4. Claim 3

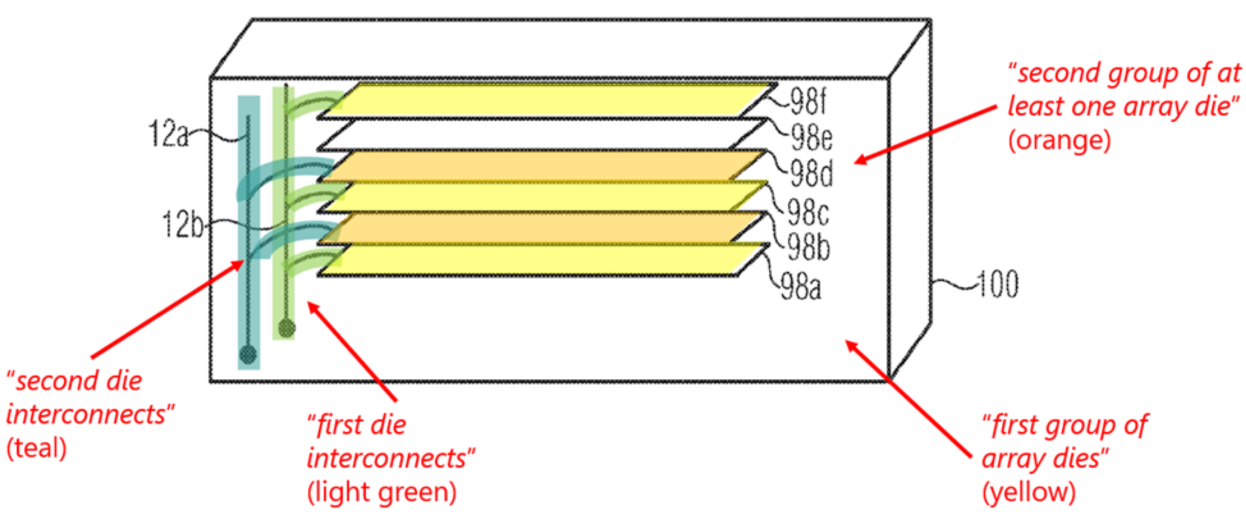
a) [3.a] Second Die Interconnects are Longer than First Die Interconnects

Ground 2 teaches "*[t]he memory package of claim 1, wherein the second die interconnects* [TS715 (teal)] *are longer than the first die interconnects* [TSV08 (light green)]," for the reasons discussed above for claim 2 (pp.101-103). EX1003, ¶¶618-624.

b) [3.b] Number of Array Dies in the Second Group is Less Than Number of Array Dies in the First Group

Ground 2 teaches "*wherein a number of array dies in the second group of at least one array die* [coupled to TSV715] *is less than a number of array dies in the first group of array dies* [coupled to TSV08]." EX1003, ¶¶625-634.

Riho teaches that "[his] invention is not limited to the above-mentioned embodiments" and could include a mix of "DRAM chips and NAND flash memory chips," EX1016, ¶¶[0135-36], while Rajan teaches that the "memory circuits" in a stack of memory devices can either be "symmetrical" or "asymmetrical" (e.g., with memories of different capacities implementing one or more ranks), EX1015, 2:62-65, 7:63-67. Thus, in the combination of Riho and Rajan in Ground 2 (pp.81-84), it would be an obvious design choice to have an "asymmetrical" stack, resulting in fewer "*array dies in the second group*" than "*in the first group of array dies*." EX1003, ¶¶629-630. Indeed, other contemporaneous references expressly disclosed such an arrangement (below), providing a further motivation for there to be fewer "*array dies in the second group*" than "*in the first group of array dies*." EX1024, 8:58-66, 9:14-18, Fig.5 (below); EX1003, ¶¶629-630.



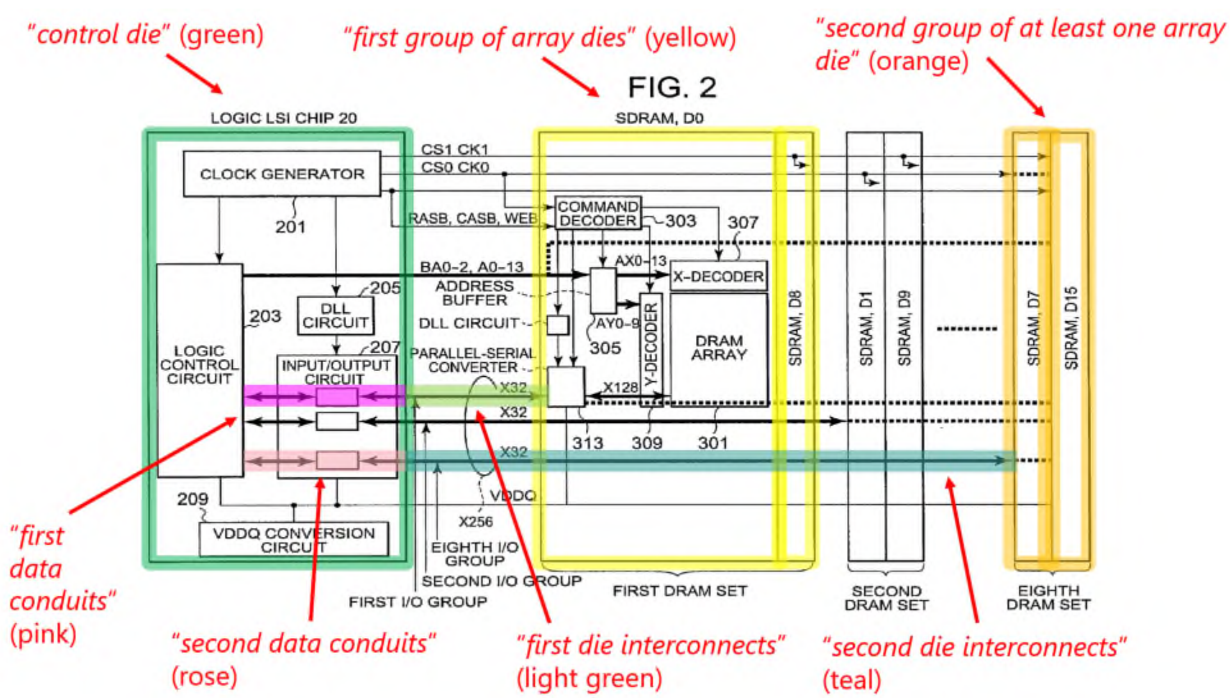
Furthermore, as discussed above (pp.6-8, 32-34), a POSITA knew that the load on a given TSV increases with the length of the TSV and with the number of dies connected to the TSV, and that driving a signal on a TSV having a larger load requires a larger driver which uses more power, and that differences in load result in timing differences (skew). EX1017, 6:15-30, 7:14-26, Figs.7-8; EX1018, ¶[0096]; EX1003, ¶631. Therefore, in an asymmetric arrangement where TSVs of different lengths are connected to different number of dies, a POSITA would have been motivated to arrange the stack in a way to reduce load and their differences: a longer TSV (e.g., TSV15 in the combination of Ground 2) is connected to fewer dies to reduce the power requirements of driving it and to avoid skew due to load differences. EX1017, 2:61-65; EX1018, ¶[0050]; EX1003, ¶632.

5. Claim 4

Ground 2 teaches "*[t]he memory package of claim 1, wherein the first driver size and the second driver size are related to a load on the first driver and a load on the second driver*," since a POSITA would have found it obvious, as explained for claim limitations [1.e.4]-[1.e.5], to follow Riho2's teaching of using different driver sizes corresponding to the different loads created by variations in the resistance and capacitance in Riho's stack. *Supra* pp.6-8, 98-101; EX1018, ¶[0097], Fig.7A; EX1003, ¶¶635-641.

6. **Claim 5**

Ground 2 teaches "*[t]he memory package of claim 1, wherein the control die* [green] *further comprises a control circuit* [including logic control circuit 203 and control circuit in input/output circuit 207, which may emulate one or more characteristics, e.g., ranks, *supra* pp.8-11, 81-84] *to control respective states* [e.g., for communicating data in the read or write direction with the correct timing] *of the first data conduits* [pink] *and the second data conduits* [rose] *in response to control signals* [e.g., read/write command signals with chip-select signals pursuant to the JEDEC standard, EX1019, pp.6-14, 18, 33] *received via the control terminals* [from an external device, as discussed for [1.b] (pp.87-90)]." EX1016, ¶¶[0039-40, 0045, 0053], Fig.2 (below); EX1003, ¶¶642-650.



Furthermore, as explained above (pp.81-84), a POSITA would have been motivated to look to Rajan for details about how Riho's control chip can interface with a host system, and Rajan discloses external terminals for control signals to read/write data according to the timing requirements in the JEDEC standards. EX1003, ¶¶646-647; EX1015, 11:12-12:13, Fig.14 (below, illustrating possible timings for read/write operations); EX1019, pp.13, 23-24 ("CAS latency"), 33.

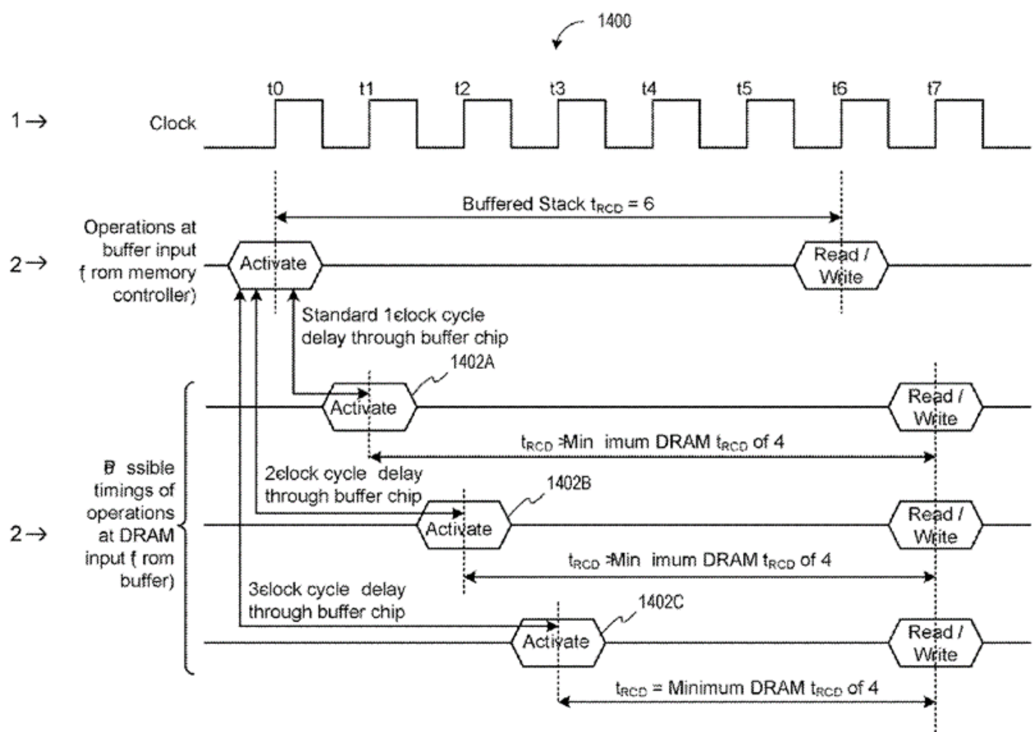


FIG. 14

7. <u>Claims 6-9</u>

The limitations of claims 6-9 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 2 for at least the same reasons discussed above:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[6.a]	[1.a]	¶¶652-655 (¶¶525-529)
[6.b]	[1.b]	¶¶656-659 (¶¶530-537)
[6.c]	[1.c]	¶¶660-662 (¶¶538-545)
[6.d.1]-[6.d.2]	[1.d.1]-[1.d.2]	¶¶663-665 (¶¶546-563)
[6.e]	[3.a]	¶¶666-668 (¶¶618-624)
[6.f]	[3.b]	¶¶669-671 (¶¶625-634)
[7.a]	[1.e.1]	¶¶673-676 (¶¶564-571)
[7.b.1]-[7.b.2]	[1.e.2]-[1.e.3]	¶¶677-680 (¶¶572-588)
[7.c.1]-[7.c.2]	[1.e.4]-[1.e.5][6]	¶¶681-683 (¶¶589-606)
[8]	[2]	¶¶684-688 (¶¶607-616)
[9][7]	[5]	¶¶689-695 (¶¶642-650)

[6] As explained above (pp.98-101), the singular "*first data conduit*" and "*second data conduit*" in [1.e.4]-[1.e.5] lack antecedent basis, but these limitations are obvious even if interpreted as plural "*first data conduit**s***" and plural "*second data conduit**s***" (like in [7.c.1]-[7.c.2]) as explained above (pp.98-101). EX1003, ¶683.

[7] In claim 9, "*the plurality of terminals*" lacks antecedent basis, but based on the surrounding claim language it appears that "*control terminals*" from [6.b] could be

8. Independent Claim 10

a) *[10.a] Preamble*

Ground 2 teaches "*[a] memory module* [e.g., including Riho's stacked memory devices, EX1016, ¶¶[0002-04], implemented in Rajan's DIMM memory module, EX1015, 1:28-32, 8:52-54, 15:3-12, Fig.8 (first below), e.g., to allow Riho's devices to be used in host systems with JEDEC-standard DIMM sockets] *operable in a computer system with a system memory controller* [e.g., Rajan's "memory controller (not shown)," EX1015, 3:5-7]*, comprising*." EX1003, ¶¶697-706; *see also* EX1022, pp.316-20 (describing "memory controller" for JEDEC-compliant systems), Fig.7.2 (second below); EX1037, Fig.1, 1:34-39 ("Memory Controller Hub (MCH)").

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the claimed "*one or more second terminals of the plurality of terminals*," making the claim obvious like claim 5. EX1003, ¶¶692-694.

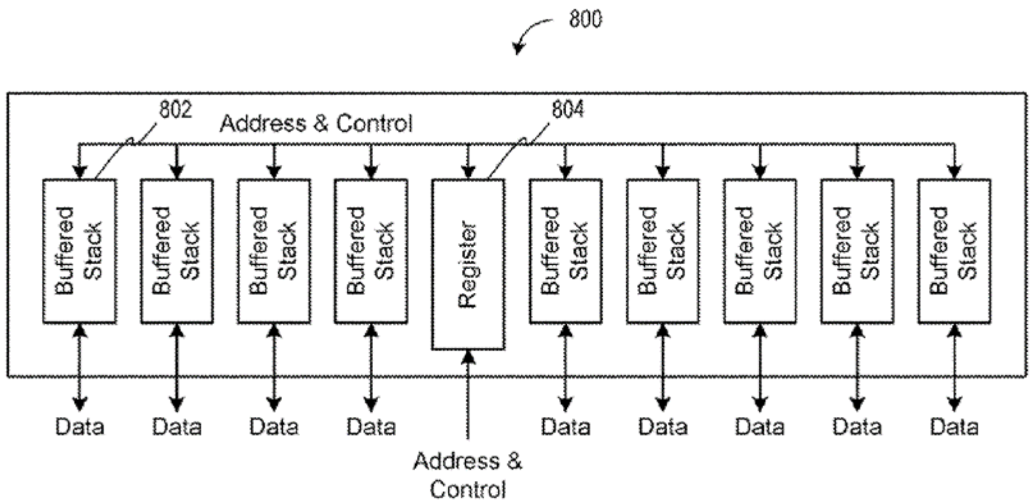


FIG. 8

316 Memory Systems: Cache, DRAM, Disk

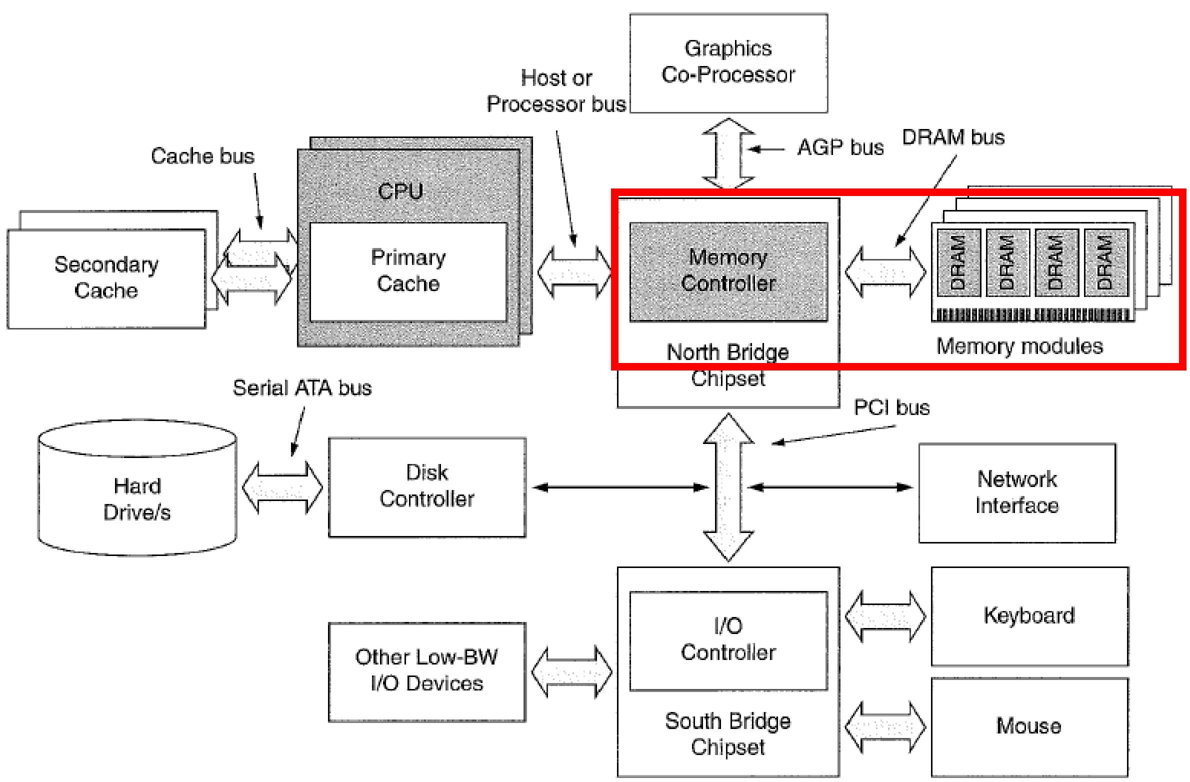


FIGURE 7.2: A typical PC organization. The DRAM subsystem is one part of a relatively complex whole. This figure illustrates a two-way multi-processor, with each processor having its own dedicated secondary cache. The parts most relevant to this report are shaded in darker grey: the CPU, the memory controller, and the individual DRAMs.

b) [10.b] A Register Device

Ground 2 teaches "*a register device* [e.g., Rajan's register 804, *see* EX1015, 8:52-58, Fig.8 (below)] *configured to receive input command/address signals* [*see id.* receiving "Address & Control" signals per the JEDEC standard, EX1015, 4:20-24, which would include command signals, *see* EX1019, pp.13, 33; EX1023, p.9, Fig.16; EX1022, pp.318-20] *from the system memory controller* [from [10.a] above] *and to output control signals* [e.g., Rajan's register outputting "Address & Control" signals (below), *see also* claim element [15.b] (pp.120-120)]." EX1003, ¶¶707-712; *see also* EX1022, pp.418-19 ("Registered Memory Module (RDIMM)").

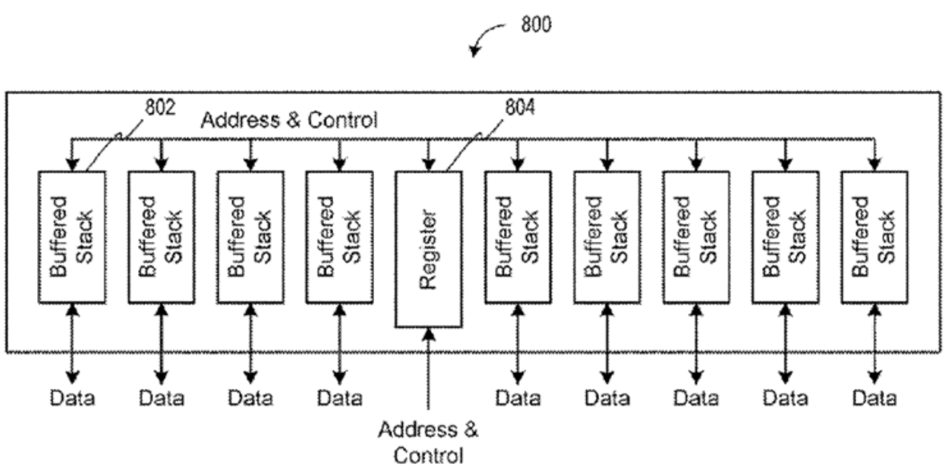


FIG. 8

c) [10.c] Plurality of DRAM Packages

Ground 2 teaches "*a plurality of DRAM packages* [e.g., buffered stacked DRAM circuits 802 (below)], *each DRAM package comprising*." EX1015, 8:52-

58, Fig.8 (below); EX1022, pp.315, 374 (DRAM "packages"); EX1016, ¶[0026], Fig.1; EX1003, ¶¶713-717.

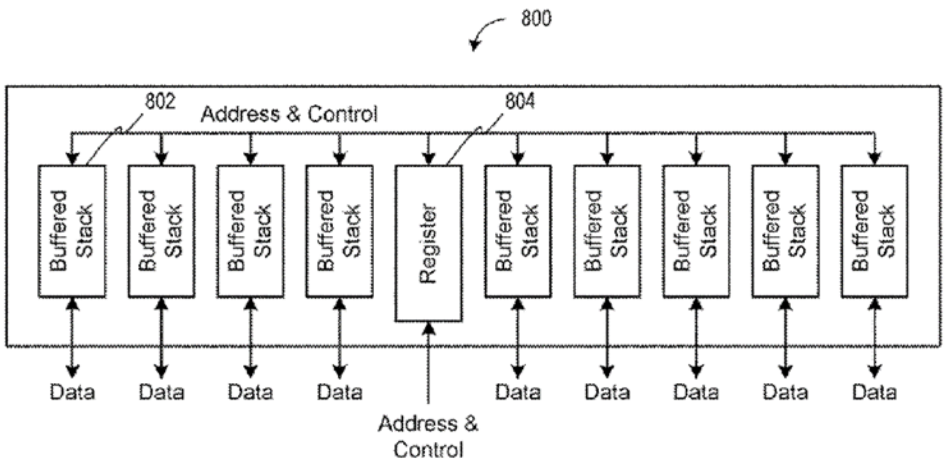


FIG. 8

d) [10.d] Data Terminals

Ground 2 teaches "*data terminals via which the DRAM package communicate data signals with the system memory controller* [as indicated below by "Data" with an arrow from the bottom of the DRAM package 802 to the system memory controller from [10.a] (pp.109-110), and as explained above for [1.b] (pp.87-90)]*, and control terminals via which the DRAM package receive the control signals from the register device* [e.g., the "Address & Control" signals from the Register 804 to the DRAM packages 802, as explained for [10.b] (pp.111-111)]." EX1003, ¶¶718-723; *see also* EX1022, pp.418-19 ("Registered Memory Module (RDIMM)"); EX1019, pp.6-13 (JEDEC standard for terminals for data, address, and control).

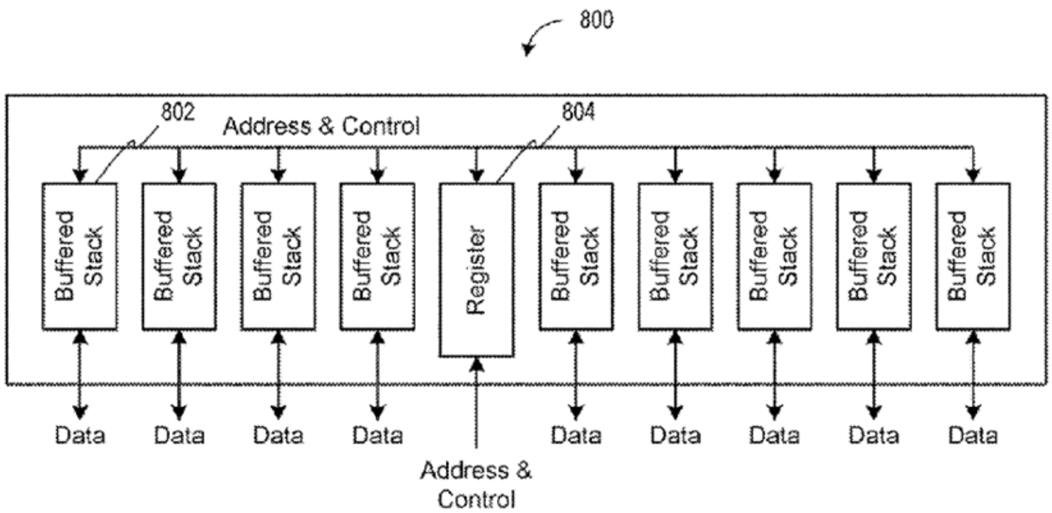


FIG. 8

e) [10.e]-[10.h.2]

The limitations [10.e]-[10.h.2] are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 2 for at least the same reasons discussed above:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[10.e]	[1.c]	¶¶724-726 (¶¶538-545)
[10.f.1]-[10.f.2]	[1.d.1]-[1.d.2]	¶¶727-729 (¶¶546-563)
[10.g.1]	[1.e.1]	¶¶730-732 (¶¶564-571)
[10.g.2]-[10.g.3]	[1.e.2]-[1.e.3]	¶¶733-735 (¶¶572-588)

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[10.h.1]-[10.h.2]	[1.e.4]-[1.e.5],[8] [10.d]	¶¶736-740 (¶¶589-606, 718-723)

9. <u>Claim 11</u>

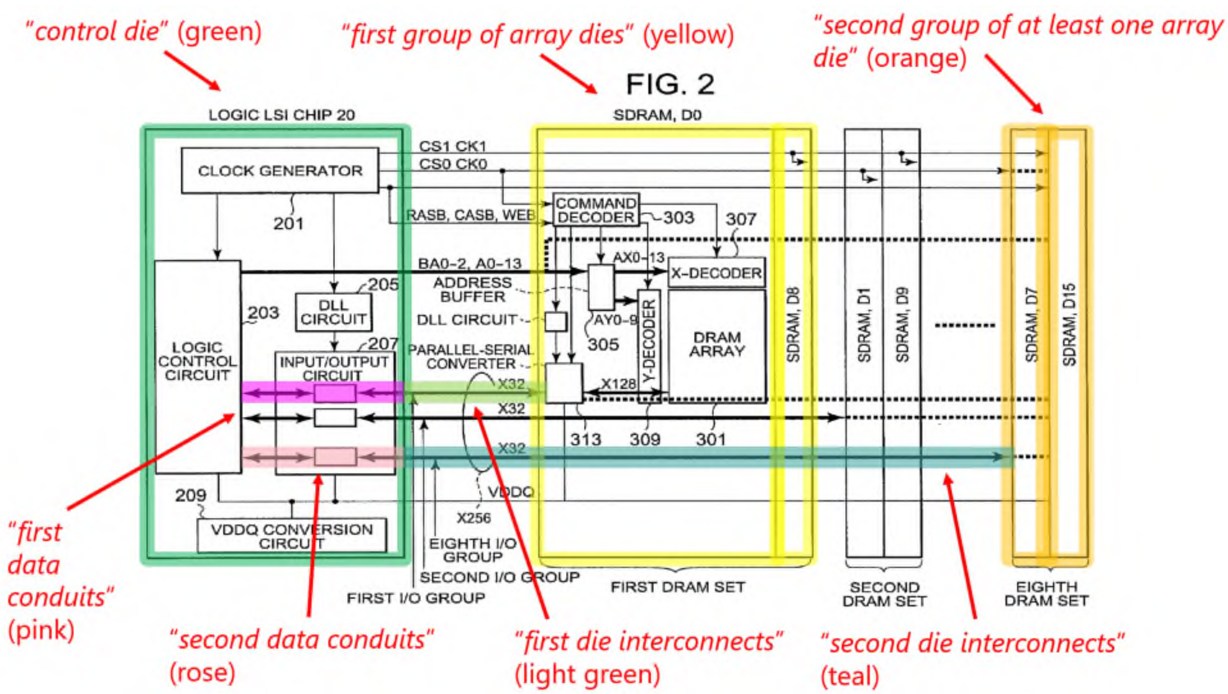
Ground 2 teaches "*[t]he memory module of claim 10, wherein the control die receives the control signals and further includes a control circuit to control respective states of the first data conduits and the second data conduits in response to the control signals*," as discussed for claim 5 (pp.106-107). EX1003, ¶¶741-744.

10. <u>Claim 12</u>

Ground 2 teaches "*[t]he memory module of claim 11, wherein the control signals* [from the "*register device*" per [10.b] (pp.111-111)] *include data path control signals generated by the register device* [e.g., chip-select and read/write command signals pursuant to the JEDEC standard, EX1019, pp.6-14, 18, 33;

[8] As explained above (pp.98-101), the singular "*first data conduit*" and "*second data conduit*" in [1.e.4]-[1.e.5] lack antecedent basis, but these limitations are obvious even if interpreted as plural "*first data conduit**<u>s</u>***" and plural "*second data conduit**<u>s</u>***" (like in [10.h.1]-[10.h.2]) as explained above (pp.98-101). EX1003, ¶738.

EX1023, p.9, Fig.16; EX1022, pp.318-20, 332-35]*, the data path control signals being used to control the respective states of the first data conduits* [pink] *and the second data conduits* [rose] [e.g., logic control circuit 203 and input/output circuit 207 (below) control the timing and direction of the data transfer (read or write) and select the die(s) for the data transfer (according to chip-select signals)]." EX1016, ¶¶[0039-40, 0045, 0053], Fig.2 (below); EX1003, ¶¶745-751. In the combination of Ground 2, either the "*control circuit*" in the "*control die*" of the memory package and/or the "*register device*" (as claimed here) can implement "rank multiplication," as discussed above (pp.8-11, 81-84), thus affecting the "*data path control signals*." EX1003, ¶749.



Furthermore, as explained above (pp.81-84), a POSITA would have been motivated to look to Rajan for details about how Riho's control chip can interface with a host system, and Rajan discloses external terminals for control signals to read/write data according to the timing requirements in the JEDEC standards. EX1003, ¶¶646-647, 748; EX1015, 11:12-12:13, Fig.14 (below, illustrating possible timings for read/write operations); EX1019, pp.13, 23-24 ("CAS latency"), 33.

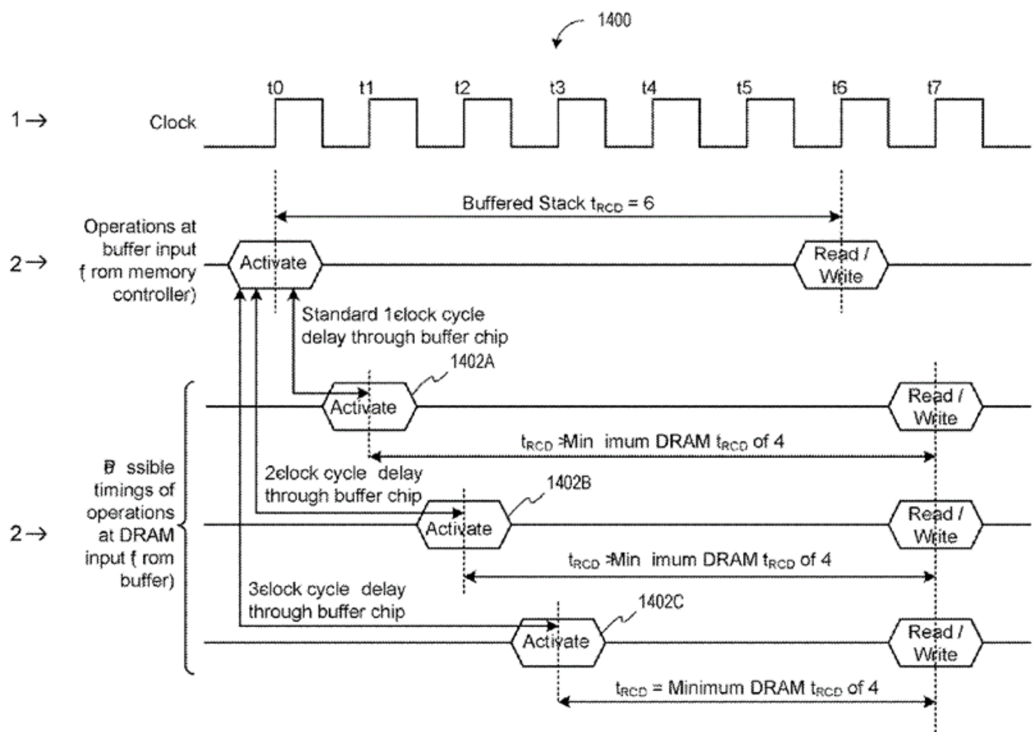


FIG. 14

11. <u>Claim 13</u>

Ground 2 teaches "*[t]he memory module of claim 11, wherein the control die* [from [1.e.1] (pp.94-95), including logic control circuit 203 and control circuit in input/output circuit 207] *is configured to generate data path control signals* [as

discussed above for claim 12 (pp.114-116), e.g., internal read/write signals, including chip-select signals pursuant to the JEDEC standard] *from at least some of the control signals* [from the "*register device*" per [10.b] (pp.111-111)], *the data path control signals being used to control the respective states of the first data conduits* [pink] *and the second data conduits* [rose] [as explained for claim 12 (pp.114-116)]." EX1003, ¶¶752-763. As discussed above for claim 12, in the combination of Ground 2, the "*control circuit*" in the memory package can also implement "rank multiplication," as discussed above (pp.8-11, 81-84), thus generating "*data path control signals*." EX1003, ¶¶760-761. In addition, as taught by Rajan, the "*control circuit*" can control the "*data conduits*" to emulate the timing and other characteristics of the JEDEC standard, as shown below. EX1015, 3:42-50, 9:46-10:27, Fig.10 (below); EX1019, pp.23-24 ("CAS latency"); EX1003, ¶¶758-759.

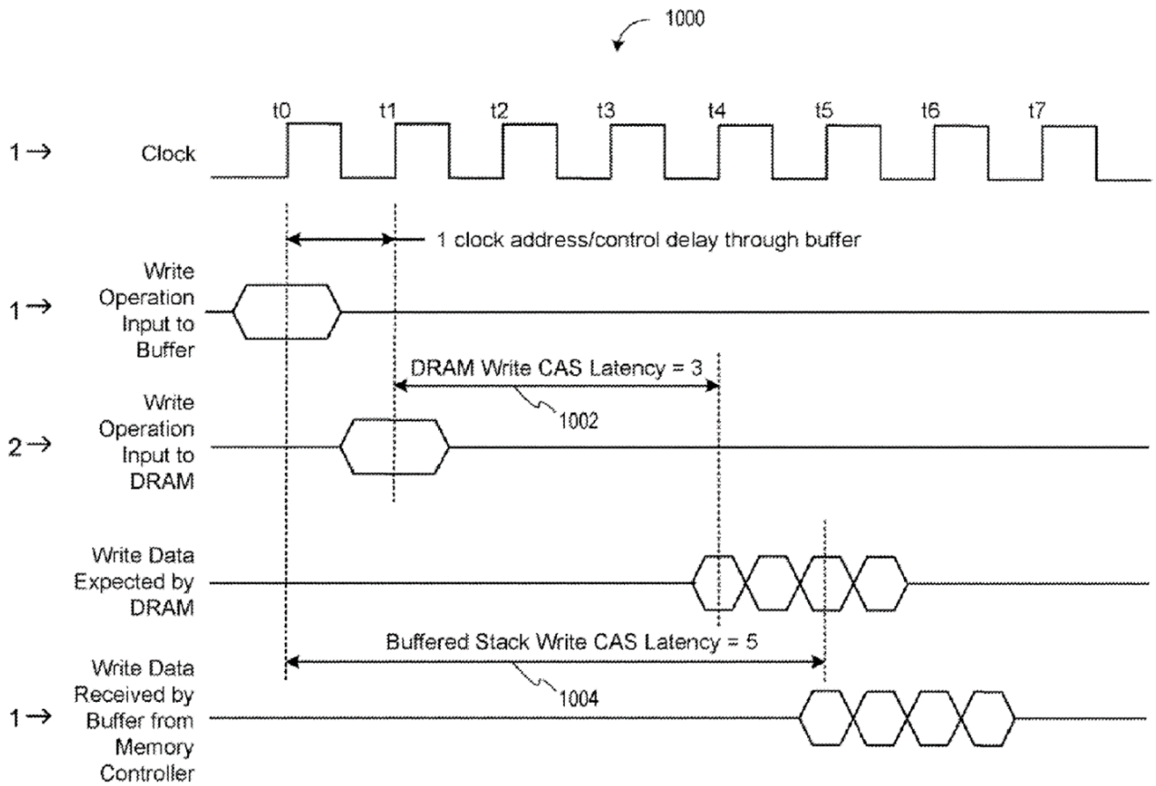


FIG. 10

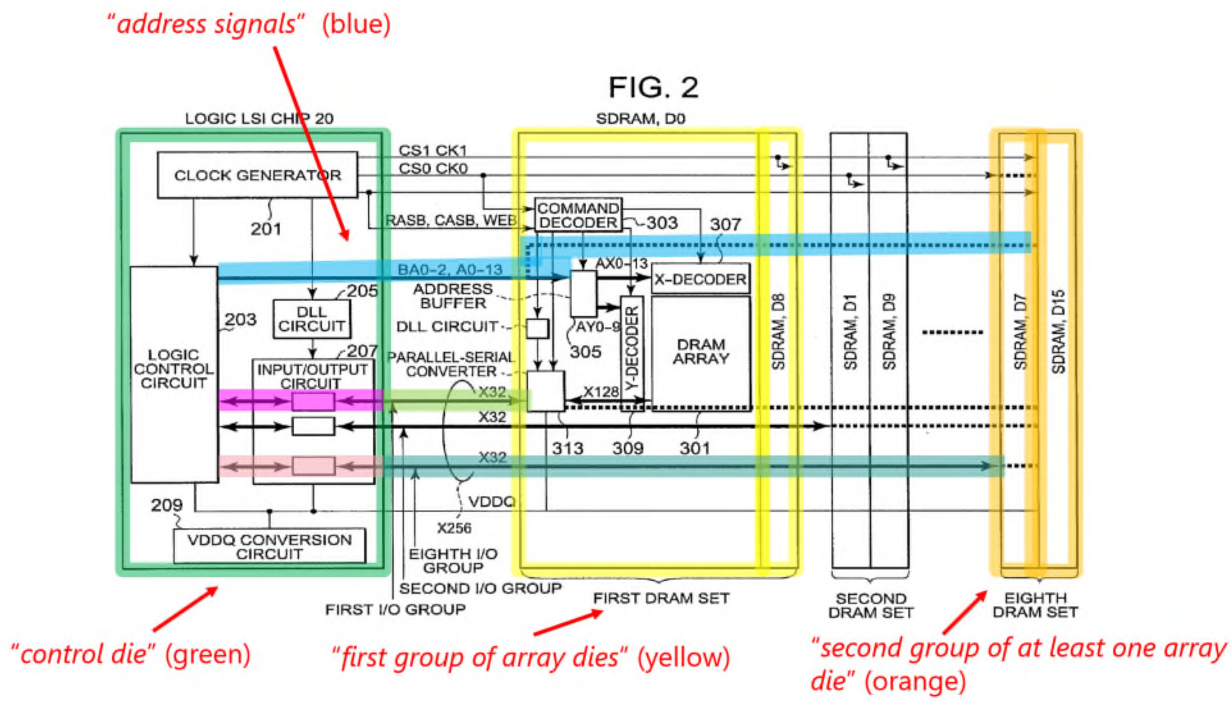
12. <u>Claim 14</u>

a) [14.a] Control Signals Include Address Signals

Ground 2 teaches "*[t]he memory module of claim 10, wherein the control signals* [from the "*register device*" per [10.b] (pp.111-111)] *include address signals* [e.g., "Address & Control" as shown in [10.b] (pp.111-111); *see also* EX1016, ¶[0039, 0043], which under the JEDEC standards for read and write commands would include address signals (e.g., A0-A15) identifying where to store or retrieve the data, *see* EX1019, pp.6-13, 18, 33; EX1023, p.9, Fig.16; EX1022, pp.318-20, 332-35]." EX1003, ¶¶765-769.

b) *[14.b] Control Die Provides the Address Signals*

Ground 2 teaches "*the control die* [green] *provides the address signals* [from [14.a] directly above, including BA0-2, A0-13 (blue, below)] *to the plurality of array dies* [e.g., D0-D15, yellow, orange]." EX1016, ¶¶[0038, 0043], Fig.2 (below); EX1003, ¶¶770-775.



13. <u>Claim 15</u>

a) *[15.a] Input Command/Address Signals Include First Chip Select Signals*

Ground 2 teaches "*[t]he memory module of claim 10, wherein the input command/address signals* [from [10.b] (pp.111-111)] *include first chip select signals* [according to the JEDEC standards, EX1019, p.13 ("[Chip Select] is

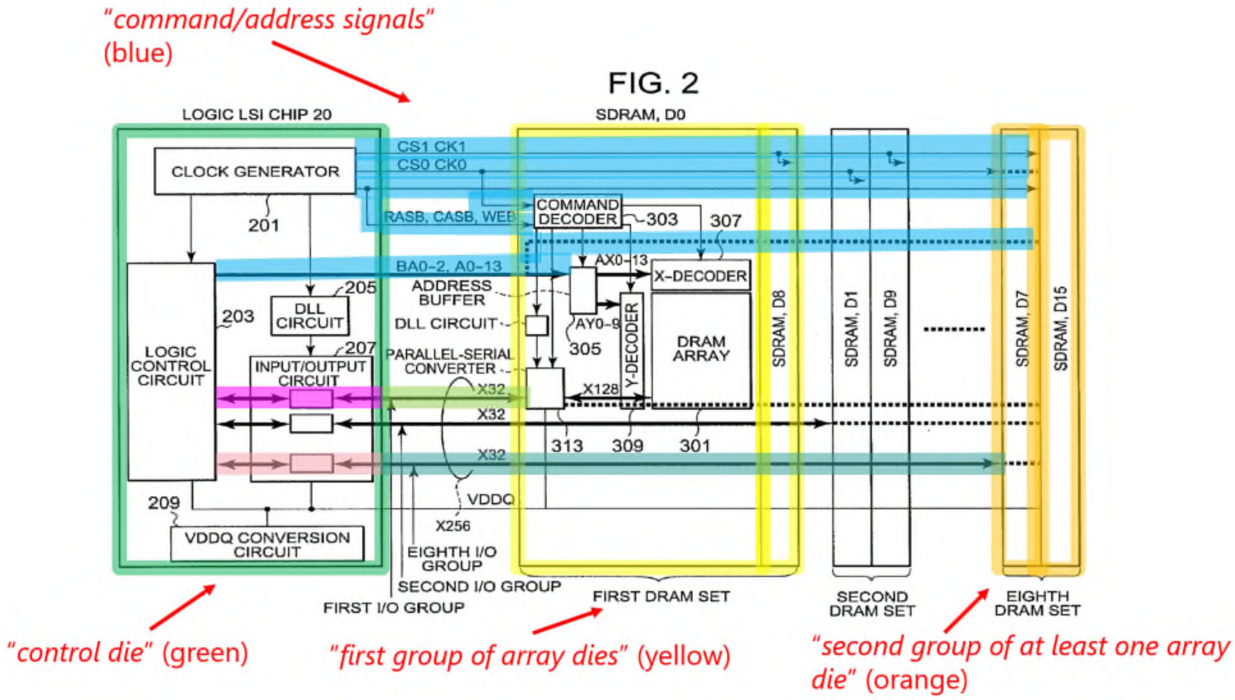
considered part of the command code")]." EX1003, ¶¶777-783; *see also* EX1015, 8:6-13.

b) [15.b] Register Device Configured to Perform Rank Multiplication

Ground 2 teaches "*wherein the register device* [from [10.b] (pp.111-111)] *is configured to perform rank multiplication by generating second chip select signals* [*see* pp.8-11 (rank multiplication); EX1015, 3:27-30; 6:30-7:67, 8:56-58 ("In one embodiment the emulation is performed at the DIMM level.")] *from at least some of the input command/address signals* [from [10.b] (pp.111-111)], *the second chip select signals having a number of chip select signals greater than the first chip select signals* [from [15.a] immediately above] *and equal to a number of array dies in the plurality of array dies* [*see* pp.8-11 (rank multiplication); EX1015, 6:34-38 (explaining that separate generated chip select signals are used for each DRAM chip in the stack)]." EX1003, ¶¶784-791. The 160 Patent also admits this was taught by the prior art. EX1001, 18:33-39, 22:19-25, Fig.7; *supra* pp.8-11.

c) [15.c] Chip Select Die Interconnects

Ground 2 teaches "*wherein the DRAM package further comprises chip select die interconnects* [e.g., <u>Riho</u>'s "TSVs" for "CS0CK0 and CS1CK1," EX1016, ¶¶[0033, 0038]] *for conducting the second chip select signals to respective ones of the plurality of array dies* [yellow, orange]." EX1003, ¶¶792-799.



It would also be obvious in light of Riho's disclosure above to include "*chip select die interconnects*" for the chip-select signals to enable read/write operations by the "*array dies*." EX1003, ¶796. Indeed, the "chip-select bus … is essential in a JEDEC style memory system," EX1022, p.319; EX1023, pp.2-4, 9, Fig.16, and the JEDEC standard required separate chip-select signals for each stacked memory chip (below, red), EX1019, pp.12-13, Fig.2 (below); EX1003, ¶796.

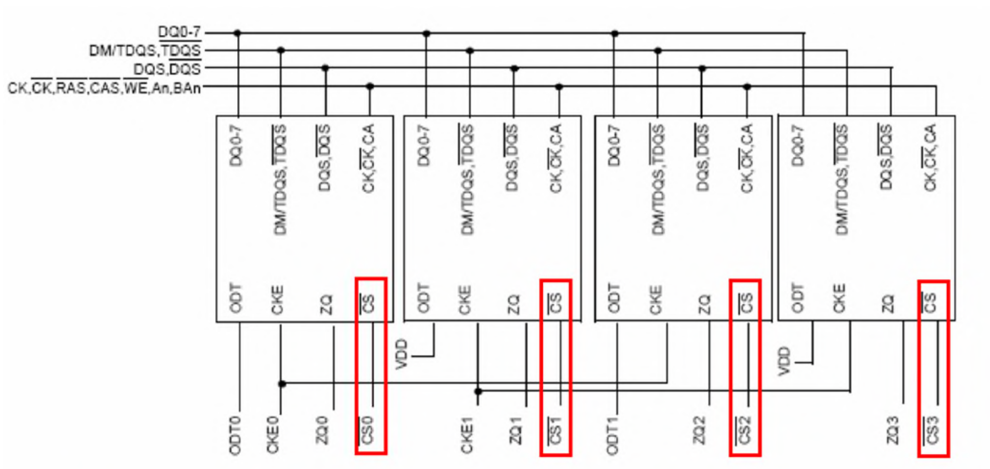


Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

Rajan further renders obvious "*chip select die interconnects*" for the chip-select signals by teaching that "extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack." EX1015, 6:34-48, Fig.4 (below); EX1003, ¶796.

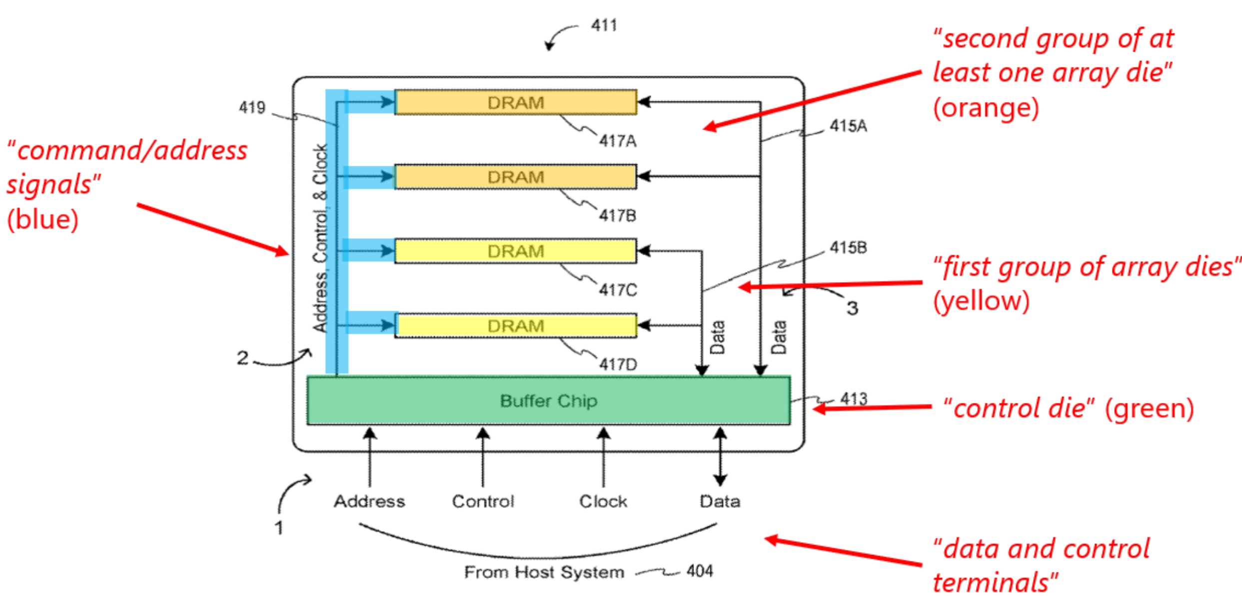


FIG. 4

The 160 Patent also admits that transmitting separate chip-select signals through "*die interconnects*" to select an "*array die*" was well-known at the time. EX1001, 1:51-58, Figs. 1A-1B; EX1003, ¶797.

14. Claim 16

a) [16.a] Control Signals Include Output Command/Address Signals Derived from the Input Command/Address Signals

Ground 2 teaches "*[t]he memory module of claim 10, wherein the control signals* [from the "*register device*" per [10.b] (pp.111-111)] *include output command/address signals derived from the input command/address signals* [e.g., received and registered by Rajan's register 804 (below) from the *system memory controller* per [10.b] (pp.111-111)], *the output command/address signals including first chip select signals* [according to the JEDEC standards, EX1019, p.13 ("[Chip Select] is considered part of the command code")]." EX1015, 8:52-58, Fig. 8 (below); EX1003, ¶¶801-807; *see also* EX1022, pp.418-19 ("Registered Memory Module (RDIMM)").

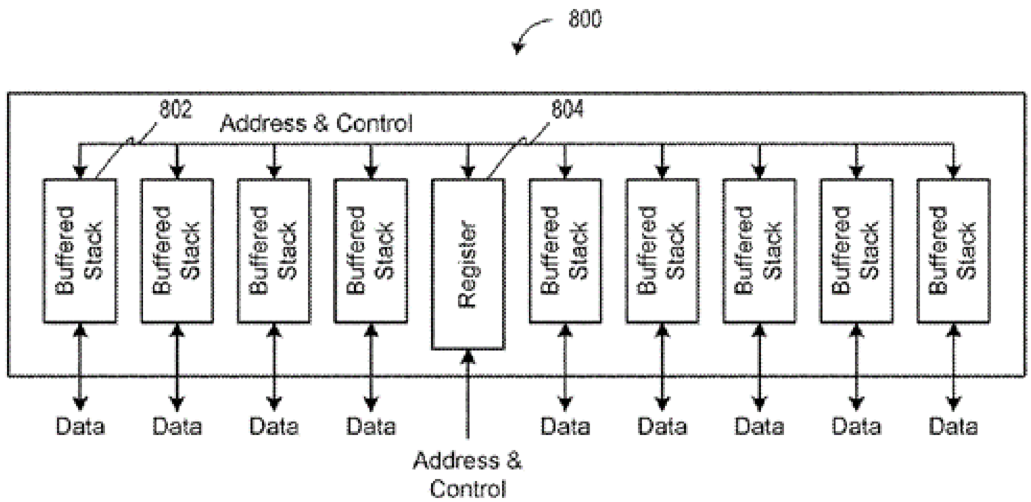


FIG. 8

b) [16.b] Control Die is Configured to Perform Rank Multiplication

Ground 2 teaches "*wherein the control die* [see [1.e.1] (pp.94-95)] *is further configured to perform rank multiplication* [see pp.8-11, 81-84] *by generating second chip select signals from at least some of the output command/address signals* [from [16.a] directly above]*, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies*," for the same reasons discussed above for [15.b] (pp.120-120), because the control circuit in the "*control die*" of Ground 2 may also implement rank multiplication (either alternatively or in addition to the register of the module), as discussed above (pp.8-11, 81-84). EX1003, ¶¶808-811; EX1015, 6:34-38 ("In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips,

utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.").

c) [16.c] Chip Select Die Interconnects

Ground 2 teaches "*wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies*," as explained for claim element [15.c] (pp.120-123) EX1003, ¶¶812-815.

15. Claim 17

Ground 2 teaches "*[t]he memory module of claim 10, wherein the first driver size and the second driver size are related to a first load on the first driver and a second load on the second driver*," as discussed above for claim 4 (p.105). EX1003, ¶¶816-820.

16. Claim 18

Ground 2 teaches "*[t]he memory module of claim 10, wherein the control signals include command/address signals* [see [10.b] (pp.111-111) and [16.a] (pp.123-124)]*, and the control die includes buffers to control the timing of the command/address signals* [e.g., Rajan's buffer chip receives command/address signals for a write command and holds those signals for "an extra two clocks of delay" to control the timing of when the stacked DRAMs receive those signals, EX1015, 9:46-10:27, Fig.11 (below)]." EX1003, ¶¶821-828. A POSITA would have been motivated by Rajan's teachings to implement this command/address

signal delay in Riho's device to emulate the characteristics of JEDEC-standard memory devices, including timing. EX1015, 9:46-10:4; EX1019, pp.23-24 ("CAS latency"); EX1003, ¶826.

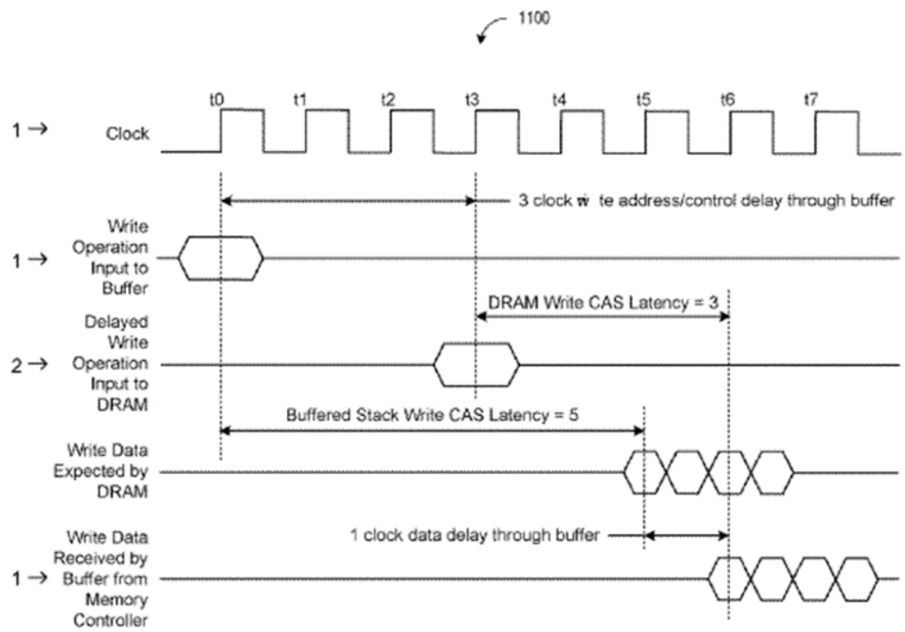


FIG. 11

17. Claim 19

Ground 2 teaches "*[t]he memory module of claim 10, wherein the control die includes data buffers to control the timing of the data signals* [e.g., by emulating a CAS latency to control the timing of data signals to and from the

DRAMs].” EX1015, 8:59-9:45, Fig.9[9] (below); EX1019, pp.23-24 (“CAS latency”); EX1003, ¶¶829-834; *see also* claim 18 (pp.125-126).

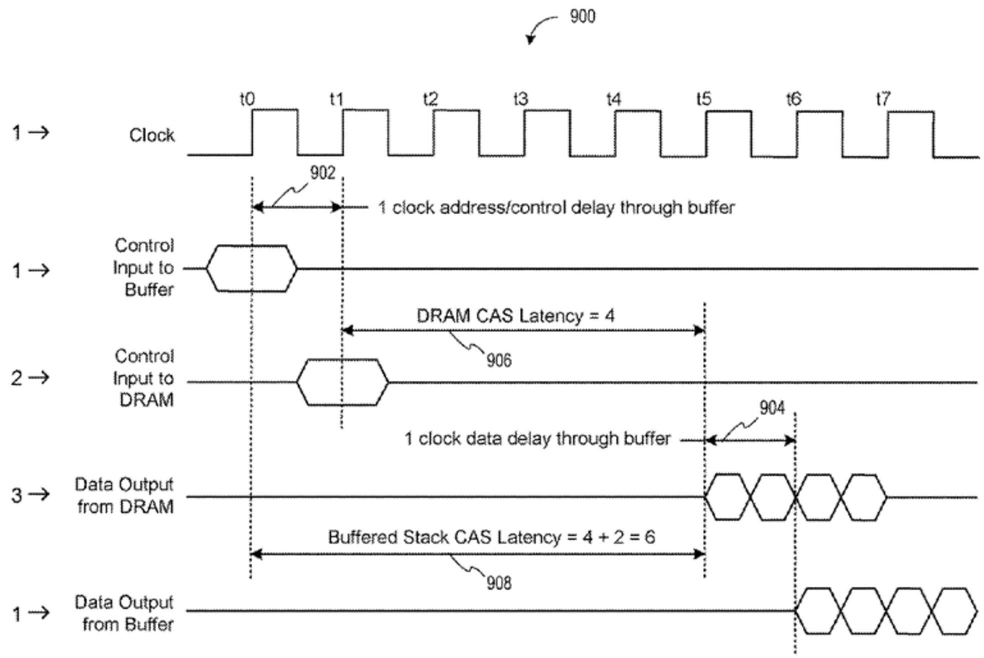


FIG. 9

18. <u>Claim 20</u>

Ground 2 teaches “*[t]he memory module of claim 10, wherein the first group of array dies include a greater number of array dies than the second group of at least one array die*,” as discussed for [3.b] (pp.103-105). EX1003, ¶¶835-839.

[9] Figure 9 contains a small typographical error showing CAS latency 908 ending at t5, instead of t6 as described in the specification. EX1015, 9:25-31; EX1003, ¶495.

VIII. §325(d)

Advanced Bionics and §325(d) do not support discretionary denial. The Examiner never considered the references asserted here (Kim, Rajan, Riho, Wyman, Riho2). Although the Examiner discussed a different reference (Rajan137) with the same inventors as Rajan during prosecution of the 060 Patent (as discussed above, p.17), the Examiner did not consider Rajan or Rajan137 in combination with the other references in Grounds 1-2 discussed above. Denial under §325(d) is thus unwarranted. *E.g.*, *Thorne Research, Inc. v. Trustees of Dartmouth College*, IPR2021-00491, Paper 18, at 8-9 (PTAB Aug. 12, 2021). Furthermore, the combinations of Grounds 1-2 clearly render obvious the limitations that Patent Owner contended were missing from Rajan137 (discussed above, p.17), including a plurality of stacked "*array dies*," and "*first*" and "*second*" "*data conduits*" in the control die, as discussed in the limitation-by-limitation analyses above.

IX. FINTIV

The *Fintiv* factors and the Interim *Fintiv* Guidance (EX1047) favor institution. There is one case currently pending between the parties involving the 160 Patent, filed in the Eastern District of Texas, which was amended in May 2022 to add the 160 Patent. EX1043-45. This petition was filed quickly, within 3 months, and the litigation with respect to the 160 Patent is just getting started. As

shown above, the merits of this petition are compelling. Thus the *Fintiv* factors favor institution. EX1047, pp.3, 8-9; EX1048, p.35; *Samsung Elecs. Co. v. Staton Techiya, LLC*, IPR2022-00324, Paper 13, at 12 (PTAB July 11, 2022) ("24.2 months"); *Siemens Indus. Inc. v. EMA Electromechanics, Inc*., IPR2021-01517, Paper 9, at 11-12 (PTAB Mar. 15, 2022) (factor 2 neutral when FWD deadline less than one month after potential trial date).

X. CONCLUSION

Petitioner therefore respectfully requests that Trial be instituted and that claims 1-20 be canceled as unpatentable.

Dated: August 26, 2022

/Eliot D. Williams/
Eliot D. Williams
Reg. No. 50,822
BAKER BOTTS L.L.P.
30 Rockefeller Plaza
New York, NY 10112
T: (212) 601-7255
F: (212) 408-2501

Theodore W. Chandler
Reg. No. 50,319
BAKER BOTTS L.L.P.
1801 Century Park East
Suite 2400
Los Angeles, CA 90067
T: (213) 202-5702
F: (213) 202-5732

Ferenc Pazmandi
Reg. No. 66,216
BAKER BOTTS L.L.P.

101 California Street
Suite 3200
San Francisco, CA 94111
T: (415) 291-6255
F: (415) 291-6355

Michael E. Knierim
Reg. No. 78,268
BAKER BOTTS L.L.P.
30 Rockefeller Plaza
New York, NY 10112
T: (212) 408-2584
F: (212) 259-2584

Brianna L. Potter
Reg. No. 76,748
BAKER BOTTS L.L.P.
1001 Page Mill Road
Building One, Suite 200
Palo Alto, CA 94304
T: (650) 739-7556
F: (650) 739-7656

Counsel for Petitioner
Samsung Electronics Co., Ltd.

CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24 because it contains 13,404 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

Dated: August 26, 2022

/Eliot D. Williams/
Eliot D. Williams
Reg. No. 50,822
BAKER BOTTS L.L.P.
30 Rockefeller Plaza
New York, NY 10112
T: (212) 601-7255
F: (212) 408-2501

Counsel for Petitioner
Samsung Electronics Co., Ltd.

CERTIFICATE OF SERVICE

I hereby certify that on this 26th day of August, 2022, a copy of this Petition, including all exhibits, has been served in its entirety by FedEx Express on the following counsel of record for Patent Owner:

Jamie J. Zheng, Ph.D., Esq.
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94306-3314

Dated: August 26, 2022

/Eliot D. Williams/
Eliot D. Williams
Reg. No. 50,822
BAKER BOTTS L.L.P.
30 Rockefeller Plaza
New York, NY 10112
T: (212) 601-7255
F: (212) 408-2501

Counsel for Petitioner
Samsung Electronics Co., Ltd.